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June 1992

PCB TESTER SELECTION FOR FUTURE SYSTEMS

ManTech Support Technology Inc.

William Schmitt

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Rome Laboratory
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Griffiss Air Force Base, NY 13441-5700

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13. ABSTRACT (Maximum 200 words)

This report describes a computer program (to run on an IBM compatible PC) designed to aid in the selection of a PCB tester, given the characteristics of the PC board to be tested. The program contains a limited data base of PCB testers, and others may be added easily.

This report also provides a specification for a limited family of PCB testers to fill the gap between what the U.S. Air Force is expected to need and what is expected to be available within the next four to six years.

The parameters used in the computer program and the specification are based on a survey of military and commercial PCBs - both those now available and those expected to come on line within the next four to six years. The results of the survey are covered in volume 2 - available from DTIC.

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EXECUTIVE SUMMARY

The Air Force's experience has been that printed circuit board (PCB) tester acquisition is a major cost driver associated with virtually every acquisition program. Without proper planning, the PCB tester acquisition can result in program cost overruns. PCB acquisition planning is made difficult by the fact that tester needs are not fully definable until the acquisition program contract has been signed. Also, maintenance policies with respect to throwaway versus repair can change, creating a need for test equipment that was unplanned and undefined. An additional difficulty is that, over the years, capabilities and technology of avionic equipment development process could not adequately address the maintenance of the new equipment at initiation or deployment.

The main product of this effort discussed in Volume 1 is the software which can be used to assist in the selection of printed circuit board (PCB) tester or testers for an electronic PCB. The inputs are the parameters on the PCB that need to be measured, and their ranges; and a database of PCB testers from which to choose. A limited database is provided with the software. The output is one of a selection of reports on the suitability of the testers selected from the database to test the PCB whose parameters were entered.

This software is available in two versions which have different databases. The first version is available to both U.S. Government agencies and qualified Government contractors. The second version contains proprietary data in the database and is available only to U.S. Government agencies. Availability of the software is discussed in Section 3.6 of Volume 1. Both the software and the User's Manual have been placed in the Defense Technical Information Center (DTIC).

Adding the desired testers to the database is relatively easy. While deleting testers is not very easy, the testers to be considered in any given situation may be selected easily.

A survey was made of current and planned PCB testers and the parameters and range of those parameters which those testers can measure. In addition, a survey was made of the technology used, or expected to be used, in current PCBs and those expected to come on line within 4 to 6 years. The output of that survey was the parameters and range of parameters which AF PCB testers will need to be able to measure within the next 4 to 6 years. From the output of these surveys, a specification discussed in Volume 1 was written defining a limited family of testers to cover the gaps between the capability of existing and planned testers and the requirements of existing and planned AF PCBs.

The details and results of the survey of AF PCB Technology are given in this volume. Basically, this consists of lists of the ranges of values required for the parameters in current and expected systems. Projections are made for some of these parameters as a function of time. Initially this is being given a very limited distribution. This volume has been placed in DTIC for those needing a copy.

1.0 INTRODUCTION

The purpose of this volume is to present the results of the Rome Laboratory PCB Tester Selection for Future Systems Study used in Volume 1. It contains the following:

- Description of the methodology used to conduct the survey of Air Force PCB Technology and current and planned PCB testers both military and commercial.

- The survey results on Air Force current PCB technology and test requirements.

- The survey results on the projections of Air Force PCB technology trends for the next four years.

2.0 EQUIPMENT AND PCB TECHNOLOGY SELECTION

This section covers the survey process used for selecting equipment and PCB technology for investigation. The electronic system and ATE data for the effort were gathered at seven sites: ManTech Support Technology, Alexandria, Virginia; Hanscom Air Force Base (AFB), Massachusetts; Kelly AFB, Texas; Robins AFB, Georgia; Griffiss AFB, New York; Grumman Melbourne Systems, Florida; and McClellan AFB, California.

2.1 CRITERIA FOR SELECTION PROCESS

Air Force avionic and related equipment investigated (contained in Appendix A) were selected for the PCB technology survey based on specific criteria. They were then analyzed to determine the test requirements of current Air Force PCB technology presented in this report. The criteria for selection were as follows:

- o The System will require Air Force support in the 1990's.
- o The System is avionic or aircraft electronic ground support equipment.
- o The System functional classification represents a unique classification category that would not otherwise be presented in this report.
- o The System has stringent test requirements which will maximize an exercise of Air Force ATE stimulus and measurability capabilities.
- o The System is from other services and has mission requirements similar to Air Force equipment.
- o The System was developed for other services but can be used by Air Force.

The process involved analyzing selected current and future Air Force avionic and related system PCB technology, PCB technology literature searches, and PCB support ATE technology data.

2.2 TECHNOLOGY AREAS SELECTED

2.2.1 PCB TEST REQUIREMENTS TECHNOLOGY AREA CATEGORIES

Test requirements technology categories were selected to provide an overview of Air Force avionic equipment and ground support test requirements in this report. They are as follows:

- o Power Requirements
- o Analog Stimulus and Measurement Requirements
- o Digital Stimulus and Measurement Requirements
- o Radio Frequency (RF) Stimulus and Measurement Requirements
- o Microwave Stimulus and Measurement Requirements
- o Synchro/Resolver Stimulus and Measurement Requirements
- o Optical Stimulus and Measurement Requirements
- o Bus Interface Requirements

2.2.2 LATEST COMPONENT TECHNOLOGIES SELECTED

To perform the trend analysis to produce test requirements of Air Force PCB enhanced technology four to six years in the future, technologies involving semiconductor materials and integrated circuit design were investigated. Based upon their current use by the commercial

electronic system designers, it is a reasonable assumption that the following components' technologies will be incorporated into future Air Force avionic and ground support equipment designs.

- o Semiconductor Material Technologies
  - Gallium Arsenide (GaAs)
  - Low Power Schottky (LS)
  - Fairchild Advanced CMOS Technology (FACT)
  - BiPolar Complementary Metal Oxide Semiconductor (BiCMOS)
- o Integrated Circuits
  - Very High Speed Integrated Circuits (VHSIC)
    - Complementary Metal Oxide Semiconductor (CMOS)
    - Integrated Schottky Logic (ISL)
    - Schottky Transistor Logic (STC)
    - GaAs
  - Millimeter Wave Monolithic Integrated Circuits (MMIC) GaAs
  - Random Access Memory (RAM)
    - GaAs
    - N-Type Metal Oxide Semiconductor (NMOS)
    - Emitter-Coupled Logic (ECL)
    - Programmable Array Logic (PAL)
    - GaAs
    - CMOS
  - Application-Specific Integrated Circuit (ASIC)
    - CMOS
    - GaAs

3.0 TECHNICAL DATA COMPILATION

3.1 IDENTIFICATION OF INFORMATION SOURCES

3.1.1 AIR FORCE AVIONIC TECHNICAL DATA SURVEY

The systems in the technical data survey were selected based upon the criteria stipulated in paragraph 2.1. The best sources of data for Air Force avionic equipment were determined to be the cognizant field activity (Air Force base), Modular Automatic Test Equipment (MATE) Users Group (MUG), or prime equipment contractors for each of the Air Force systems for which they provide system maintenance support.

3.1.2 ATE TECHNICAL DATA SURVEY

The data sources identified for ATE technical data are the following:

- o Technical Orders for military ATE
- o ATE vendors
- o ATE specifications
- o ATE users both military and commercial
- o Military ATE internal investigation studies.

3.1.3 DEFENSE TECHNICAL INFORMATION CENTER (DTIC)

DTIC, under the auspices of the Department of Defense, provides a technical service by maintaining a database of defense related reports including research studies. These research

studies are available to qualified users upon request. In this manner, DTIC provides an excellent data source for information regarding military Research and Development (R&D) efforts and technology.

DTIC performs data searches for the Government and its contractors based upon a requested subject. Each search is organized into a bibliography with an abstract for each report title. A client then simply reviews each report abstract and determines which report he desires to order. For a minimal fee the DTIC provides a complete copy of any report required.

These reports cover a wide spectrum of electronic subjects such as microprocessors, computers, solid-state technology, millimeter, RF technology, fiber optics, and spread spectrum.

3.1.4 TRADE JOURNALS LITERATURE SEARCH

As the electronic industry has progressed, trade journals (e.g., Electronics, Electronic Design, Military Electronics, Institute of Electrical and Electronic Engineers (IEEE) Publications) have been a recognized source of technical data regarding the latest technologies. These journals often carry articles about electronic technology and provide annual technology forecasts which are helpful with technical information. Books and reports soon become dated due to the rapid advances being made in electronic technology. Thus, the journal articles provide the most current source of technical data.

3.1.5 RELEVANT COMPANY STUDIES

Since our company has performed similar studies, prior company contracts in allied areas were reviewed to determine if any material in those reports could be helpful. Of

particular interest was the company report by William J. Schmitt, "Supplement Technology Trend Analysis and Test Requirements Final Report," which was prepared for the Naval Electronic Systems Engineering Center, San Diego and referenced in Appendix D, page D-7.

3.1.6 TRADE CONFERENCES

Trade conferences have been excellent sources of information for the latest technology, built-in test, and ATE test program development techniques. The various trade meetings organized by the IEEE have been a particularly useful source of technical papers and reports in the past. Consequently, a necessary step in preparation of this report was to select appropriate trade conferences that would provide pertinent data in the technical area being studied.

3.1.7 NEW TECHNOLOGY SURVEY

A key approach used in generating the final report's technology projection is the conducting of a technology survey. The survey data sources for this report were identified as MUG members; prime equipment contractors; ATE vendors; trade conference attendees; and ManTech clients, both Government and commercial.

3.2 DATA COLLECTION

Following the identification of the data sources, the important task of collecting the pertinent technical data on ATE and avionic electronic equipment was initiated. The approach taken to acquire the information from each of the data sources is described below.

3.2.1 TECHNICAL SURVEY

The selected Air Force data sources referenced in Section 3.1. were first contacted by phone through the MATE points of contact. After obtaining the name of the point of contact at each Air Force base, the necessary Rome Laboratory (RL) letter was sent stating the purpose of the survey and requesting permission to visit each site.

To collect the technical data, a team of two engineers was used. One engineer interviewed cognizant equipment managers and engineers. This enabled us to obtain information on the facility's ATE capabilities. This information was recorded on the PCB Tester Survey Form (as shown in Appendix B). The second engineer concurrently reviewed PCB documentation (i.e., schematics, test requirements documents, calibration and maintenance manuals, repair specifications) and recorded it on the PCB Data Sheet (as shown in Appendix C).

3.2.2 DEFENSE TECHNICAL INFORMATION CENTER (DTIC)

3.2.2.1 TECHNOLOGICAL SEARCH PROCESS

Since the DTIC database is enormous, it was necessary to narrow the search by selecting pertinent topics for the purpose of projecting technology trends and test requirements. The topics chosen were microprocessors, testing methods, VHSIC, test requirements, technology trends, and MMIC. The search covered the period from 1980 to the present. A list was obtained of relevant reports with their abstracts.

3.2.2.2 REPORT SELECTION PROCESS

The listing supplied by DTIC was reviewed by reading the abstracts to determine which reports warranted further investigation. Further investigation involved ordering copies of the pertinent reports, reviewing items, and selecting those relevant to the projected technology trends and test requirements. The bibliography contained in Appendix D lists the reports selected.

3.2.3 TRADE JOURNALS

3.2.3.1 RESEARCH

The research commenced with acquiring back issues of trade journals from 1987 through February 1991. Each journal listed below was reviewed for technical articles germane to the study.

- Electronic Design
- Microwave & RF
- Electronic Test
- IEEE Computer
- EDN
- Computer Design
- Digital Design
- Evaluation Engineering
- Mini-Micro System
- Electronics
- Electronic Products
- Defense Electronics
- VLSI Design
- Solid State Technology
- Research and Development
- Military Electronics

3.2.3.2 ARTICLE SELECTION

Articles selected for inclusion in Appendix D were chosen for their relevance to the following topics:

- Digital Technology Forecast and R&D Efforts
- Digital Testing
- Military VHSIC Program
- New Digital Components
- Microprocessors and Microprocessor Peripherals
- Digital Buses
- Microprocessor Based Systems
- Military MMIC Program
- Analog Testing
- New Analog Components
- Analog to Digital (A/D) and Digital to Analog (D/A) Converters
- Analog Technology Forecast and R&D Efforts
- Artificial Intelligence

3.2.4 MANTECH RELATED STUDIES AND REPORTS

3.2.4.1 RESEARCH

An extensive search was conducted throughout ManTech to identify any previously contracted studies relating to technology trends and test requirements. All such reports performed after 1980 were reviewed for pertinence to this study.

3.2.4.2 STUDIES AND REPORT SELECTION

ManTech studies and reports were included if they were germane to any of the following technical areas:

- o Microprocessors
- o Microprocessor Based Systems
- o Analog and Digital Technology
- o Testing Equipment Requirements
- o Artificial Intelligence
- o RF Technology

3.2.5 ADVANCED TECHNOLOGY SURVEY

3.2.5.1 TYPE OF SURVEY

Many approaches for conducting technical surveys have been devised. They include telephone interviews, mailed questionnaires, and personal interviews. Mailed questionnaires to be filled in by respondents (even those who agreed ahead of time) often create problems. The questionnaires, if returned at all, are often not returned in a timely fashion. Also, a certain degree of ambiguity is almost always associated with written questions. It is never possible to anticipate all the areas a respondent may believe are important and may want to discuss. Consequently, the written questionnaire cannot be sufficiently flexible for all respondents.

The questionnaire (as listed in Appendix E) was mailed to MUG members and/or followed up by telephone and in-person interviews. This technique has been used over the last decade in many studies for Governmental and commercial organizations. These interviews offered flexibility and proved timely, compared to written questionnaire answers.

3.2.5.2 GROUP SURVEYED

Conducting an informal group survey was one of the primary methods used to obtain data regarding existing ATE at military test sites (as listed in Appendix F) and analog and digital technology projections (as listed in Section 6.0). The surveys were conducted at trade conferences (e.g., International Test Conference and AUTOTESTCON) and at military and industrial installations during the data collection phase. ManTech's past experience regarding technology use by Government and commercial clients has also been included as a part of the survey.

The surveyed data was compiled from personnel from the following facilities:

- Griffiss AFB
- AEGIS Program Office (Navy)
- LANTIRN Program Office (Air Force)
- JSTARS Program Office (Air Force)
- Martin Marietta
- Robins AFB
- Harris Corporation
- Grumman Corporation
- ManTech International Corporation

- McClellan AFB
- Hanscom AFB
- Kelly AFB
- Teradyne Incorporated
- GenRad Inc.
- Hewlett Packard Company
- General Electronics Company

3.2.5.3 PROCEDURES

Over an eight month period, some 50 interviews were conducted regarding current and future PCB digital and analog technology. Those interviewed were chosen by recommendation of key government ATE personnel working in the MATE program offices, system program offices at Air Force bases, and at Air Force development centers. Often the MATE focal point was used as the initial point of contact, and the MATE focal point scheduled the interview with the Government to avoid conflicts. In all cases, those recommended were people with ATE experience.

The purpose of the interviews was to gain insight into the digital and analog electronic technology from the present to 1996 time frame.

The informal interview was conducted along certain guidelines. Those interviewed were asked to discuss present technology of their equipment and, if possible, technology upgrades to their equipment. They were asked on what assumptions they based their projections. They were asked to identify additional technical issues and what effect those issues would have on test requirements. Most important, they were asked for any pertinent comments. That is, they

were given the opportunity to voice their concerns, insights, and ideas. The results of the survey have been summarized and integrated with the data obtained from other sources and used for the technology projections shown in Section 6.0 of this final report.

3.3 DATA ORGANIZATION

3.3.1 DATA CATEGORIES

As technical data was gathered, it was divided into one of two major categories, commercial or military data. The sources for the data are as follows:

- Military Data Sources
  - Air Force Calibration Maintenance and Repair Specification
  - Air Force Equipment Survey Data
  - Military Journals
  - Military Technical Orders and Schematics
  - Military Technical Reports and Test Requirements Documentation

- Commercial Data Sources
  - Trade Journals
  - Conference Proceedings and Publications
  - Commercial Industry Survey
  - ATE Commercial Equipment Specifications
  - ATE Brochures

3.3.2 PERTINENT DATA SELECTION AND RECORDING

After the technical data was categorized as military or commercial, each individual data item was reviewed. Passages or paragraphs pertinent to PCB technology and ATE were selected and duly recorded. The recording involved creating a computer listing identifying the source, title, author, and page number(s) applicable. This listing was used to form a database which served as the report bibliography which is contained in Appendix D.

3.4 DATA COMPREHENSIVENESS REVIEW

3.4.1 REVIEW

With the database organized, a comprehensive review was conducted. The database was reviewed to verify coverage of the following key technologies:

- Digital Components Characteristics
- RAM Characteristics
- Bus Architecture
- Integrated Circuit Power Dissipation
- Integrated Circuit Gate Delay
- RF Components
- Optical Devices
- Synchro and Resolver Integrated Circuits
- Analog Integrated Circuits
- Power Supply Characteristics
- MMIC Program

- o VHSIC Program

3.4.2 RESULTS

The database was found to be generally sufficient. However, in some cases, the documentation of military systems, particularly the optical systems, lacked sufficient available data to perform detailed test requirements analysis. In order to fill the voids caused by this lack of military data, systems similar to the military systems were used. Care was taken to ensure that the substitute "commercial equivalent" systems employed were similar to the Air Force technology.

4.0 TECHNOLOGY ANALYSIS

4.1 ANALOG

4.1.1 POWER

An important part of any electronic system is the power source. Without it, the system cannot operate. Unfortunately, a power source can add unwanted heat, size, and weight to the system design. Consequently, integrated circuits (IC's) are often selected in PCB designs to accommodate a common low voltage in order to reduce supply requirements and power consumption. According to the data collected, the most common IC operating voltages used in PCB design are ±5V, ±12V, ±15V, ±24V, and ±28V dc. Also observed from the data is that current Air Force system PCB designers are minimizing system power consumption through the use of CMOS technology wherever appropriate. CMOS devices draw less current than BIPOLAR, ECL, GaAs, and NMOS. However, minimizing system power is accomplished at the expense of speed.

Another technique that reduces power requirements is the digitizing of formerly analog functions which also supports the general trend to lower system voltages. However, the front end of many systems still requires voltage levels of 100V and higher. Tables 4-1 and 4-2 show the analytical results from the survey data regarding current PCB/modular power supply parametric characteristics.

TABLE 4-1 CURRENT PCB DC POWER SUPPLY PARAMETRIC CHARACTERISTICS

VOLTAGE RANGE	MAXIMUM CURRENT	MINIMUM VOLTAGE TOLERANCE *	MINIMUM VOLTAGE RIPPLE *
0 Vdc - 5 Vdc	10.0 A	50.0 mV	20.0 mV
5.1 Vdc - 12 Vdc	4.0 A	50.0 mV	50.0 mV
12.1 Vdc - 15 Vdc	1.0 A	0.5 V	50.0 mV
15.1 Vdc - 24 Vdc	3.0 A	1.0 V	100.0 mV
24.1 Vdc - 30 Vdc	12.0 A	1.0 V	500.0 mV
30.1 Vdc - 50 Vdc	1.0 A	1.0 V	500.0 mV
50.1 Vdc - 100 Vdc	0.1 A	2.5 V	500.0 mV
OVER 100 Vdc	0.1 A	5.0 V	1.0 V

* Reference Appendix L Glossary of Terms for definition

TABLE 4-2 CURRENT PCB AC POWER SUPPLY PARAMETRIC CHARACTERISTICS

VOLTAGE RANGE	MAXIMUM CURRENT	FREQUENCY	VOLTAGE IMBALANCE	PHASE CONFIGURATION
0 Vac-100 Vac	1.5 A	60/400 Hz	± 5%	Single Phase 3 Phase Wye 3 Phase Delta
101 Vac-250 Vac	10.0 A	60/400 Hz	± 5%	Single Phase 3 Phase Wye 3 Phase Delta

4.1.2 CIRCUITRY

Current analog (non-RF) technology components are becoming more accurate, stable, and compact and have better performance capabilities than their predecessors. The discrete component (e.g., transistor, resistor, relay, application specific circuitry) is being replaced by

IC's (e.g., resistor packs, Operational Amplifiers (OP AMPs), multiplexers, ASIC's, transistor packs) which can represent several components or even entire circuits. This results in reduced real estate requirements as compared to the equivalent discrete component analog circuitry.

However, the functional operations of analog circuitry remains essentially unchanged. The technology still involves oscillators, amplifiers, modulators, power supplies, pulses and demodulation. On the other hand, on the basis of the data collected, it appears that analog technology is being replaced in many systems with digital technology by use of A/D's and D/A's, which allow today's PCB design engineers to take advantage of digital design techniques. This process, which is known as digitization, allows system PCB designs which reduce the size of the system, improve signal-to-noise ratio, and increase signal processing speed. However, as stated previously, the front end of many systems will remain analog in order to interface with the analog (real) world. Table 4-3 presents the results of the analysis of the data collected.

4.1.3 RF/MICROWAVE TECHNOLOGY

RF/Microwave technology, as with analog technology, is presently going through a transition period in which integrated circuit technologies such as ASIC, VHSIC, and MMIC are replacing discrete component circuit designs, and solid-state devices are replacing tube technology. In addition, small and medium scale integrated circuits used in system designs of the 1970's and early 1980's are being replaced with larger scale integrated circuits and VHSIC wherever possible in system design upgrading.

TABLE 4-3 OVERVIEW OF CURRENT AIR FORCE AND RELATED ELECTRONIC EQUIPMENT ANALOG TECHNOLOGY

ANALOG SIGNAL TYPE	PARAMETER	RANGE VALUE
PRECISION DC VOLTAGE STIMULUS	Output Voltage	0 to ±100 V
PRECISION DC CURRENT STIMULUS	Output Current	0 to 200 mA
VOLTAGE STIMULUS	Frequency Amplitude	0.083 Hz to 10 MHz 0.4 to 20 Vp-p
DC VOLTAGE MEASUREMENT	Voltage	0.1 Vdc to 2000 Vdc
VOLTAGE MEASUREMENT	Voltage Frequency	0.884 Vac to 450 Vac 0.083 Hz to 10 MHz
CURRENT MEASUREMENT	Current Frequency	0.1 Arms to 3.8 Arms 60 Hz to 400 Hz
RESISTANCE MEASUREMENT	Resistance	3.1 Ohms to 1 MOhms
PROGRAMMABLE ACTIVE LOAD	Current Limit Maximum Power	0.1 A to 1.6 A 50 Watts
WAVEFORM STIMULUS	Waveform Type: Amplitude DC Offset Frequency Duty Cycle	-- Sine -- Square -- Triangle -- Ramp 0.05 Vp-p to 20 Vp-p 0.0 Vdc to 10.0 Vdc 0.025 Hz to 60 MHz 20 % to 80 %
PULSE STIMULUS	Frequency Pulse Width Rise Time Fall Time Amplitude Burst Length	0.625 Hz to 60 MHz 10 ns to 1 s 5 ns to 20 ms 5 ns to 20 ms 0.1 to 5.0 Vp-p 1 to 2000

TABLE 4-3 OVERVIEW OF CURRENT AIR FORCE AND RELATED ELECTRONIC EQUIPMENT ANALOG TECHNOLOGY (Continued)

ANALOG SIGNAL TYPE	PARAMETER	RANGE VALUE
ARBITRARY SIGNAL STIMULUS	Frequency Seg./Waveform Seg./Duration Amplitude	0.125 Hz to 10 MHz 3 to 100 Segments 1 μs to 1.11 ms 0.1 Vp-p to 7.7 Vp-p
FREQUENCY MEASUREMENT	Frequency	0.016 Hz to 40 MHz
WAVEFORM AMPLITUDE MEASUREMENT	Amplitude Frequency	0.1 Vp-p to 20 Vp-p 1 Hz to 10 MHz
PERIOD MEASUREMENT	Period Amplitude	18 μs to 1 s 0.1 Vp-p to 4.0 Vp-p
PULSE WIDTH MEASUREMENT	Pulse Width Amplitude	4 μs to 20 ms 0.1 Vp-p to 5.1 Vp-p
DUTY CYCLE MEASUREMENT	Duty Cycle Frequency	8.3 % to 80.0 % 1 Hz to 1.536 MHz
RISE TIME MEASUREMENT	Rise Time Amplitude	12 ns to 123 ms 2 Vp-p to 10 Vp-p
FALL TIME MEASUREMENT	Fall Time Amplitude	2 μs to 200 ms 2 Vp-p to 10 Vp-p
SLEW RATE MEASUREMENT	Slew Rate	0.6860 V/s*
TIME DELAY MEASUREMENT	Time Delay	5 ns to 20 s
EVENT COUNT MEASUREMENT	Event Count	446 to 65,536
RELATIVE PHASE MEASUREMENT	Relative Phase	120 to 240 Degrees

* Only one equipment surveyed specified this parameter

Overall, the current RF/microwave technology is still performing the same fundamental functions as its predecessor (e.g., amplification, modulation, transmission, detection) in the functional Air Force categories listed below:

- o Offensive
- o Defensive
- o Communication
- o Identification
- o Navigation

The most dramatic change with the greatest impact seen taking place in the RF/microwave technology is digitization. The result is that hybrid PCB's and modules are becoming more common in the RF/microwave technology system. Based on the data collected, Table 4-4 presents an overview of the fielded Air Force electronic equipment RF/microwave technology.

TABLE 4-4 OVERVIEW OF FIELDED AIR FORCE ELECTRONIC EQUIPMENT RF/MICROWAVE TECHNOLOGY

INPUT/OUTPUT (I/O)	PARAMETERS	RANGE
INPUT	Frequency	15 kHz to 26.5 GHz
	Power Level	-133 dBm to +41.5 dBm
	Modulation Type	AM, FM, SSB, DSB, and Pulse
	Digital Data Rate	200 Hz to 10 MHz
OUTPUT	Frequency	15 kHz to 26.5 GHz
	Power Level	-117 dBm to + 40 dBm
	Modulation Type	AM, FM, SSB, DSB, and Pulse
	Digital Data Rate	200 Hz to 10 MHz

4.1.4 SYNCHRO/RESOLVER

There was no evidence in the Air Force or commercial data collected to suggest that synchro/resolver technology performance has changed much over the years, particularly from the 1980's to the present. This technology is so specialized that the only changes that occurred involved basically the packaging of the synchro/resolver circuitry. Currently, there exist synchro/resolver integrated modules of printed circuit boards that are designed by specialty synchro/resolver companies.

The synchro/resolver technology performance overview, gathered from the data collected, is presented in Table 4-5 below.

TABLE 4-5 OVERVIEW OF CURRENT AIR FORCE ELECTRONIC EQUIPMENT SYNCHRO/RESOLVER TECHNOLOGY

UUT INTERFACE INPUT/OUTPUT (I/O)	PARAMETER	RANGE VALUE
INPUT	Frequency	50 Hz to 400 Hz
	Formats:	3-Wire Synchro
		4-Wire Resolver
	Amplitude	11.8, 26, or 90 Vrms
	Angles	0 to 360 Degrees
OUTPUT	Frequency	50 Hz to 400 Hz
	Formats:	3-Wire Synchro
		4-Wire Resolver
	Amplitude	11.8, 26, or 90 Vrms
	Angles	0 to 360 Degrees

4.1.5 OPTICAL

Today with advancements being made in communications and weapons systems through the use of optical technology, lightwave frequency systems are finding broader military

applications. These advancements are a direct result of research conducted in optical technology.

In communications, optical technology research has involved the use of semiconductor lasers as signal sources and the improvement in transmission using fiber optics (e.g., glass) rather than metal as the transmission medium. The elimination of metal transmission lines provides low loss, wide bandwidth and noninductive transmission without crosstalk; and produces a highly insulated, thin, and lightweight cable. Accordingly, a tenfold increase in both the distance between relay stations and the information content has become possible. The military has exploited these advantages for both high volume communications and long distance transmission without the use of relay stations.

In weapon systems, optical technology research has involved the use of magnifying glasses, lenses, and concave mirrors to tighten the already coherent, narrow beam of light to an even finer point. As with other technologies, optical devices have been developed to include stabilized light sources, modulation, demodulation, filter attenuators, and signal detectors.

For both the communication and weapons systems, research has found the laser to be the most useful light source because of its stability, intensity, directionality, coherence, and bandwidth. These properties enable the laser light beam to be modulated for communication systems and to perform location and measurement functions for a weapon system. There are basically four types of lasers which are briefly described below.

Solid State - This type of laser is made from a solid rod of crystalline material such as ruby. The impurities in the ruby, such as chromium, emit coherent radiation when stimulated

by a strong white light. The yttrium aluminum garnet (YAG) doped with neodymen is another form of laser which emits in the same way.

Gas - Gas lasers rely on colliding atoms transferring energy to create lasing action. The process starts with some of the atoms of the gas being excited by pumping in energy using an electrical discharge. When these excited gas atoms hit other unexcited (ground state) atoms, a transferring of energy takes place between them, causing an increase in the number of excited atoms. Another application of energy at this time with the proper frequency knocks the excited atoms back to a lower energy level, forcing them to emit coherent photons. These photons zigzag back and forth between mirrors until lasing action occurs. One of the mirrors is partially transparent and allows some light to emerge as a laser beam. Common types of gas used are carbon dioxide, argon, helium-rem and krypton.

Liquid - These lasers use a "cell" of liquid nitrobenzene to block the mirror shutter of a ruby laser. This "cell" absorbs the light and re-emits it as coherent light at a different wavelength. Liquid lasers are special because they are tunable.

Semiconductor - To make a semiconductor laser work, a Positive-Negative (PN) junction is "doped" and energized. When the current flows through the PN junction, the excess electrons in the N-region cross the junction to the holes in the P-region. As the electrons drop into the holes, they change energy levels giving off a photon. With the two sides of the semiconductor crystal polished, the photons bounce back and forth and laser action results.

Because of developments in laser technology, optical technology has progressed to accommodate these lasers and their applications. These applications include the following key military equipment classifications:

- Range Finders
- Gyroscopes
- Radars
- Communication Systems
- Weapon Systems

Optical devices have progressed to the point where the I/O communication parameters, shown in Table 4-6 below, are typical.

TABLE 4-6 OVERVIEW OF CURRENT SOLID-STATE OPTICAL COMMUNICATION TECHNOLOGY

SIGNAL TYPE	UUT INTERFACE I/O	PARAMETER	RANGE VALUE
OPTICAL SIGNAL	Input	Wavelength Amplitude Modulation	0.76 μm to 1.8 μm -10 dBm to +3 dBm AM, Pulse, FM
OPTICAL SIGNAL	Output	Wavelength Amplitude Modulation	0.76 μm to 1.8 μm -9 dBm to +10 dBm AM, Pulse, FM

Also in recent years, networking has become more and more prevalent in our information-oriented society while, at the same time, an increase in the amount and transmission rate of information is needed. Thus, data storage techniques and data transmission techniques are becoming the focus of much current research in order to increase volume, reduce access time, and increase data rates for information handling systems and networks. Many researchers see optical technology as the answer to meeting this need.

Consequently, today we are seeing more and more off-the-shelf fiber-optic equipment and laser disk technology being integrated into new systems and networking designs. Some of the off-the-shelf fiber-optic equipment being used today are transmitters and receivers modules which provide the system designer with a cost-effective way to significantly improve data-link transmission performance. The performance of these modules covers a spectrum of data rates that extends from dc to the gigabit-per-second range. Bit error rates of 10^{-9} or better are commonplace with distances in the kilometer range, while Electromagnetic Interference/Radio Frequency Interference (EMI/RFI) problems are minimized.

At the low end of the data rate spectrum, fiber optic transmitters and receivers are handling computer interfaces by replacing conventional hardware in Electronic Industries Association Recommended Standards (EIA-RS) EIA-RS-232 and EIA-RS-422 format asynchronous data links. These transmitters and receivers operate typically in the ranges specified below:

OPTICAL OUTPUT POWER:	30 nW to 950 mW
OPTICAL INPUT SENSITIVITY:	-45 dBm to -38 dBm
BAUD:	dc to 1 Megabits-per-second (Mb/s)

At the high end of the data rate spectrum, fiber-optic transmitters and receivers provide a different set of parameters to handle digital applications and are well suited for analog and video services in applications involving workstation and security transaction links. These transmitters and receivers operate typically in the ranges specified below:

OPTICAL OUTPUT POWER:	10 μW to 100 μW
OPTICAL INPUT SENSITIVITY:	-31 dBm to -10 dBm

BAUD:	10 Mb/s to 1.7 Gigabits-per-second (Gb/s)
OPTICAL PULSE WIDTH:	20 ns to 50 ns
OPTICAL RISE/FALL TIME:	4 ns to 25 ns

Because of recent advances in speed and voltage ratings of optocouplers, there is also a widespread use of optocouplers in such applications as motor controls, process control, power supplies, data transmissions, compact disc players, video disc players, and telecommunications equipment. The typical characteristic parameters for current optocouplers are:

EMITTER WAVELENGTH:	660 nm to 940 nm
ISOLATION VOLTAGE RATING:	7,500 V
BAUD:	40 b/s to 1 Mb/s

Currently in the optical storage area, the Write Once/Read Many (WORM) drive subsystems are being used. This technology provides today's system designers with mass storage capabilities which are described below:

STORAGE CAPABILITY:	200 Megabytes (Mbytes) to 1.2 Gigabytes (Gbytes)
ROTATIONAL SPEED:	334 rpm to 1,800 rpm
AVERAGE ACCESS TIME:	65 ns to 230 ns
BURST THROUGHPUT:	2.5 Mb/s to 5 Mb/s
POWER CONSUMPTION:	12 Watts to 115 Watts

4.2 DIGITAL

Over the past two decades, progress in digital technology has received the most attention because existing Air Force ATE has been strained to perform adequate testing and fault diagnostics. Digital technology has been perceived as having the greatest impact on Air Force test requirements because of the advent of the 4 bit to the 32 bit microprocessor based boards.

Even more today, with further Air Force digital technology enhancements, more off-the-shelf commercial digital equipment and digitizing of analog functions, digital test requirements continue to receive the most attention. However, current analog technology will also strain existing Air Force ATE, and analog test requirements will continue to exist during the 1990-1996 time frame. Table 4-7 presents an overview of the current Air Force digital technology baseline. It is based on available Air Force electronic equipment and commercial data.

In order to meet the needs of new technology, the Department of Defense (DoD) has revamped the VHSIC Program Phase II to produce IC's with 0.5μm geometries instead of the original planned 0.8μm geometries. These geometries will allow companies to build "superchips" (approximately 35 million transistors). Thus, there is room to carry spare parts on IC's for repairs. Concurrently, the DoD's MMIC program is looking into developing IC's with 0.25μm geometries which can operate in the GHz frequency ranges.

With the advent of Very Large Scale Integration (VLSI), microprocessors, and networking, bus technology is the cornerstone of system design. Notably, microprocessors are being used for built-in-test (BIT), control, and data processing where the bus is used to tie

together internal functions and to interface with external equipment. The most common equipment buses used today are described in Table 4-8.

TABLE 4-7 OVERVIEW OF CURRENT AIR FORCE AND RELATED EQUIPMENT DIGITAL TECHNOLOGY

COMPONENTS OR PCB TYPE	PARAMETER	RANGE VALUE
MICROPROCESSOR	Clock Frequency	1 MHz to 33 MHz
	Data Rate	100 kb/s to 50 Mb/s
	Word Length	4 to 32 Bits
	Instruction Cycle Time	250 μs to 50 ns
	Memory Size	256 Bytes to 64 kBytes
RAM	Memory Size	1 kBits to 64 kBits
	Access Time	80 ns to 250 ms
Dynamic Random Access Memory(DRAM)	Memory Size	1 kBits to 16 kBits
	Access Time	80 ns to 200 ms
	Refresh Rate	1 kHz to 100 kHz
Read-Only Memory (ROM)	Memory Size	1 kBits to 64 kBits
	Access Time	120 ns to 500 ms
Programmable Read-Only Memory(PROM), Electrically Programmable Read-Only Memory(EPROM)	Memory Size	256 Bits to 32 kBits
	Access Time	150 n to 300 ms
Electrically erasable/ Programmable Read-OnlyMemory(EEPROM)	Memory Size	2 kBytes to 16 kBytes
	Access Time	150 ns to 300 ns
VLSI, LSI, ETC. PCB	Number of Simultaneous Inputs	256 Pins maximum
	Number of Simultaneous Outputs	256 Pins maximum
	Number of Bi-Directionals	512 Pins maximum
	Stimulus Voltage	-28 V to +28 V
	Response Voltage	-28 V to +28 V
	Sink Current	3 to 50 mA
	Source Current	3 to 50 mA
	Number of Logic Families	1 to 3 Families
	Clock Rate	100 kHz to 60 MHz
	Data Skew	1 ns to 100 ns
	Rise/Fall Time	1 ns to 50 ns
	Number of Power Supplies	1 to 5 Supplies
	Power Supply Voltage Range	-30 V to +30 V
	Serial Word Length	4 to 32 Bits
	Dynamic Interface Timing:	
	Cycle Length	100 ns to 100 μs
	Drive Phases per Cycle	No data
	Test Windows per Cycle	No data
	Timing Delay	No data
	Data Format	NR[1],R0[2],R1[3],RZ[4],RC[5]

1. NR - Non Return
2. R0 - Return to Zero
3. R1 - Return to 1
4. RZ - Return to Hi-Z
5. RC Return to Complement

TABLE 4-8 CURRENT COMMON DATA BUSES

BUS NAME	TYPE	FORMAT	DATA RATE
MIL-STD-1553	SERIAL	3 BIT SYNC, 16 DATA BITS, 1 PARITY BIT	1MHz
EIA-RS-232	SERIAL	2 DATA, 5 TO 13 CONTROL LINES, 8 BIT WORD	20 kHz
CURRENT LOOP	SERIAL	START BIT, 8 DATA BITS, 1 OR 2 STOP BITS	ASYNCH. (EST. 9600 b/s MAXIMUM (MAX.))
EIA-RS-449	SERIAL	2 DATA, 2 TIMING, 4 CONTROL LINES, 8 BIT WORDS	ASYNCH. (10 M BAUD MAX.)
DEC UNIBUS	PARALLEL	16 DATA, 18 ADDRESS, 122 CONTROL	1.5 MHz
INTEL MULTIBUS	PARALLEL	16 DATA, 16 ADDRESS, 9 INTERRUPTS, 2 CLOCKS, 11 CONTROLS	ASYNCH. (5 Mwords/SEC. MAX.)
VME	SER./PARALLEL	32 DATA, 32 ADDRESS, 7 INTERRUPTS, 2 CLOCKS, 26 CONTROLS, 6 ADDRESS MODIFIERS	
ETHERNET	SERIAL	56 PREAMBLE, 8 START FRAME DELIMITEX, 16 OR 48 DESTINATION ADDRESS, 16 OR 48 SOURCE ADDRESS, 16 LENGTH, 8 N(LLC), 8N+ ADDRESS SIZE + 48 (PAD), 32 FRAME CHECK SEQUENCE	1 Mb/s to 20 Mb/s
FIBER OPTIC	SERIAL	EIA-RS-232 FORMAT	1 Mb/s to 1.7 Gb/s

5.0 TEST REQUIREMENTS ANALYSIS

5.1 ANALOG

The analog technology of the selected Air Force equipment covered technology from dc to microwave (GHz) range. Generally, the current analog technology dictates test requirements that are unchanged from earlier technologies in terms of basic analog test functions to be performed. However, the analysis indicates there has been an increase in the number of high frequency equipment, board complexities, hybrid circuits, and increased performance accuracies of equipment.

Consequently, the familiar analog test instruments are still necessary. However, their performance accuracies must be greater, and supporting ATE systems must meet more stringent performance requirements at the Unit Under Test (UUT) interface than predecessor systems in order to accommodate current analog parametric requirements. As for the hybrid circuits, the test requirement is to provide some digital interface capability as part of the analog interface in order to avoid the use of active devices in the Interface Test Adaptor (ITA). This digital interface is described in Table 5-1 along with analog functional test requirements. Unfortunately, the survey data made available was not sufficient to determine required accuracies of the stimulus and measurement test requirements.

5.2 DIGITAL

This study has revealed that Air Force equipment is incorporating current technology in its latest system design using such components as 32 bit microprocessors, large ROM, large

TABLE 5-1 CURRENT ANALOG TEST REQUIREMENTS

ANALOG SIGNAL TYPE	PARAMETER	RANGE VALUE
PRECISION DC VOLTAGE STIMULUS	Voltage	0 to ±100 V
PRECISION DC CURRENT STIMULUS	Current	0 to 200 mA
AC VOLTAGE STIMULUS	Frequency Amplitude	0 Hz to 10 MHz 0 Vp-p to 20 Vp-p
DC VOLTAGE MEASUREMENT	Voltage	0 Vdc to 2000 Vdc
AC VOLTAGE MEASUREMENT	Voltage Frequency	0 Vac to 450 Vac 0 Hz to 10 MHz
AC CURRENT MEASUREMENT	Current Frequency	0.1 Arms to 5 Arms 60 Hz to 400 Hz
RESISTANCE MEASUREMENT	Resistance	0.1 Ohms to 10 MOhms
PROGRAMMABLE ACTIVE LOAD	Current Limit Maximum Power	0.1 A to 3 A 50 Watts
WAVEFORM STIMULUS	Waveform Type: Amplitude DC Offset Frequency Duty Cycle	-- Sine -- Square -- Triangle -- Ramp 0.01 Vp-p to 20 Vp-p 0.0 Vdc to 10.0 Vdc 0.025 Hz to 60 MHz 0.1 % to 99.9 %
PULSE STIMULUS	Frequency Pulse Width Rise Time Fall Time Amplitude Burst Length	0 Hz to 60 MHz 1 ns to 1 s 1 ns to 20 ms 1 ns to 20 ms 0.1 to 5.0 Vp-p 1 to 5000

TABLE 5-1 CURRENT ANALOG TEST REQUIREMENTS (Continued)

ANALOG SIGNAL TYPE	PARAMETER	RANGE VALUE
ARBITRARY SIGNAL STIMULUS	Frequency Seg./Waveform Seg. Duration Amplitude	0 Hz to 10 MHz 2 to 100 Segments 1 ns to 100 ms 0.1 Vp-p to 10.0 Vp-p
FREQUENCY MEASUREMENT	Frequency	0 Hz to 100 MHz
WAVEFORM AMPLITUDE MEASUREMENT	Amplitude	0.1 Vp-p to 20 Vp-p
PERIOD MEASUREMENT	Period Amplitude	1 ns to 1 s 0.1 Vp-p to 10.0 Vp-p
PULSE WIDTH MEASUREMENT	Pulse Width Amplitude	1 ns to 100 ms 0.1 Vp-p to 10.0 Vp-p
DUTY CYCLE MEASUREMENT	Duty Cycle Frequency	0 % to 100 % 1 Hz to 50 MHz
RISE TIME MEASUREMENT	Rise Time Amplitude	1 ns to 200 ms 2 Vp-p to 10 Vp-p
FALL TIME MEASUREMENT	Fall Time Amplitude	1 ns to 200 ms 2 Vp-p to 10 Vp-p
SLEW RATE MEASUREMENT	Slew Rate	0.1 V/s to 100 V/s
TIME DELAY MEASUREMENT	Time Delay	1 ns to 20 s
EVENT COUNT MEASUREMENT	Event Count	1 to 100,000 Counts
RELATIVE PHASE MEASUREMENT	Relative Phase	0 to 360 Degrees
RF SIGNAL STIMULUS	Frequency Output Power Impedance	10 MHz to 26.5 GHz -60 dBm to +40 dBm 50 Ohms

TABLE 5-1 CURRENT ANALOG TEST REQUIREMENTS (Continued)

ANALOG SIGNAL TYPE	PARAMETER	RANGE VALUE
PHASE MODULATED STIMULUS	Carrier Freq. Output Power Impedance	10 MHz to 26.5 GHz -133 dBm to 0 dBm 50 Ohms
PULSE MODULATED STIMULUS	Carrier Freq. Output Power Mod. Pulse Rate Pulse Width Impedance Voltage Standing Wave Ratio (VSWR)	10 MHz to 26.5 GHz -100 dBm to +40 dBm 200 Hz to 100 kHz 500 ns 50 Ohms 1.5 : 1 Maximum
RF POWER MEASUREMENT	Power Frequency Impedance VSWR	-100 dBm to +40 dBm 15 kHz to 26.5 GHz 50 Ohms 1.5 : 1 Maximum
SPECTRUM ANALYSIS	Freq. Range Impedance	15 kHz to 26.5 GHz 50 Ohms
MODULATION ANALYSIS	Mod. Type: Carrier Freq. Power Impedance	-- Amplitude -- Frequency -- Phase -- Pulse 15 kHz to 26.5 GHz -100 dBm to 0 dBm 50 Ohms
SYNCHRO/ RESOLVER SIMULATOR	Output Format: Digital Input Frequency Amplitude	-- 3 Wire Synchro -- 4 Wire Resolver 0 to 360 Degrees 60/400 Hz 11.8/26/90 Vrms
SYNCHRO/ RESOLVER INDICATOR	Output Format: Digital Output Frequency Amplitude	-- 3 Wire Synchro -- 4 Wire Resolver 0 to 360 Degrees 60/400 Hz 11.8/26/90 Vrms

TABLE 5-1 CURRENT ANALOG TEST REQUIREMENTS (Continued)

ANALOG SIGNAL TYPE	PARAMETER	RANGE VALUE
VIDEO STIMULUS	Video Format:	-- NTSC[1] -- SECAM[2] -- PAL -- EIA-RS-375 -- EIA-RS-343/170
	Amplitude	1.0 Vp-p
VIDEO MEASUREMENT	Video Format:	-- NTSC -- SECAM -- PAL -- EIA-RS-375 -- EIA-RS-343/170
	Amplitude	1.0 Vp-p
DIGITAL PIN REQUIREMENTS	Simultaneous Logic Sets	1 to 3 Sets
	Pins Per Logic Set	1 to 200 Pins
	Driver Pins	1 to 256 Pins
	Sensor Pins	1 to 250 Pins
DIGITAL DRIVERS	Logic Lo	-30.0 V to +0.4 V
	Logic Hi	+4.0 V to +30.0 V
	Max. Sink	50 mA
	Max. Source	50 mA
DIGITAL SENSORS	Logic Lo	-30.0 V to +0.8 V
	Logic Hi	+2.4 V to +30.0 V
DIGITAL CLOCK	Frequency	10 kHz to 30 MHz
	Duty Cycle	1 % to 99 %

1 NTSC - National Television System Committee
2 SECAM - Sequential Color and Memory

TABLE 5-1 CURRENT ANALOG TEST REQUIREMENTS (Continued)

ANALOG SIGNAL TYPE	PARAMETER	RANGE VALUE
SERIAL BUS INTERFACE	Interface Type:	-- MIL-STD-1553 A/B -- ETHERNET -- SCSI[3] -- EIA-RS-232 -- EIA-RS-422
	Data Rate	75 b/s to 12 Mb/s
	Bits Per Word	71 Bits
	Start Bits	1 Bit
	Stop Bits	1 Bit
	Parity Type:	-- EVEN -- ODD -- NONE
NON-FORMATTED DIGITAL	Pattern Rate	10 kHz to 60 MHz
	Burst Length	1,500 Patterns
	Dynamic Mem. Refresh	YES
FORMATTED DIGITAL	Timing Set Duration	100 ns to 100 μs
	Drive Phase Resolution	5 ns
	Data Format:	-- NR, R0, R1, -- RZ, RC
OPTICAL STIMULUS	Wavelength	0.76 μm to 1.8 μm
	Amplitude	-10 dBm to +3 dBm
	Modulation	AM, Pulse, FM
OPTICAL MEASUREMENT	Wavelength	0.76 μm to 1.8 μm
	Amplitude	-9 dBm to +10 dBm
	Modulation	AM, Pulse, FM

3 SCSI - Small Computer System Interface

RAM, A/D converters, D/A converters, and video IC's. The IC's being used in Air Force equipment are becoming larger, and larger scale IC's make the PCB's more difficult to test. The use of ROM IC's indicates that embedded software (firmware) is becoming prevalent in the latest Air Force equipments. As for digital clock rates, 100MHz, as indicated in other studies performed by ManTech, remains the near term digital technology goal.

It was also evident from the systems reviewed and the technical interviews performed that, over the years, there were three components which had a major impact on the design of today's digital systems and subsequent digital test requirements. They were the microprocessor, analog-to-digital converter, and digital-to-analog converter. These three components have made it possible to integrate computer power with weapon and communication systems to make them smart and allow them to communicate with the real world (analog). Consequently, a revolution in the electronics industry has actually taken place where the thrust is to digitize analog functions whenever possible because digital circuits provide the following advantages over analog circuits:

- o Higher signal to noise ratio
- o Less distortion
- o Simpler design
- o Ease of design using Computer Aided Design (CAD) tools
- o Better maintainability
- o Less power consumption

Beside these three components, this revolution has been aided by the advent of very large scale digital IC's (e.g., memories, management, co-microprocessors) which have greatly reduced component count and have allowed the packaging of powerful electronic systems to

get smaller or denser. It appears that this packaging process is only in its infancy. In light of these achievements, it is important that the Air Force meet digital test requirements by providing adequate testing facilities for both current and future technology.

Table 5-2 lists the key digital test requirements for the Air Force's latest and near term electronic technology as derived from the technical interviews and system data collected.

TABLE 5-2 CURRENT DIGITAL TEST REQUIREMENTS

SIGNAL	STIMULUS/ RESPONSE	PARAMETER	RANGE VALUE
I/O	Bidirectional	Pin count	512
CLOCK RATE	Stimulus	Frequency	60 MHz
DATA RATE	Bidirectional	Frequency	0-60 MHz
PIN MEMORY	Bidirectional	Word depth	1 M
LOGIC LEVEL I/O	Bidirectional	Voltage Static	0 to $\pm$30 V
		Voltage Dynamic	0 to $\pm$15 V
		Sink/source Current	0 to 50 mA
		Data Skew	1 to 100 ns
		Rise/fall time	0.5 ns
		Logic Family Mix	0.1 ns
		(simultaneously)	3 types
		Dynamic Interface Timing:	
		Cycle Length	100 ns to 100 μs
		Drive Phases per Cycle	No data
		Test Windows per Cycle	No data
		Timing Delay	No data
		Data Format	NR, R0, R1, RZ, RC

6.0 TECHNOLOGY TRENDS

6.1 GENERAL

The results of the future technology survey conducted through the questionnaire mailing to the MUG, magazine article searches, military base visits, and industry interviews are presented in this section.

Future military PCB technology depends upon today's IC technology because past experience has shown it takes five to seven years for new technology to be used in military equipment. Thus, in order to forecast PCB technology trends, the IC technologies must be studied since future PCB designs are not available. However, the IC technology, of which the PCB components are made, determines the PCB's performance capabilities.

6.2 ANALOG

6.2.1 POWER

Until recently, power supply designs have changed very little over the years. However, in the next four to six years, the nature of power supplies will change more and more due to a conjunction of technology trends driven by innovation and predicated on the continuing displacement of linear-designed power supplies with switching-regulated supplies in moderately priced equipment, and the downscaling of equipment size requirements. These changes are triggered by power supply designers' sensitivity to the harmony that must exist between design and production to allow the translation of ideas into reliable, cost-effective power supplies. Fortunately the downscale of power supply size to accommodate the reduction of equipment

size is complemented by another trend to reduce power consumption of electronic components powered by these supplies. Figure 6-1 on page 6-3, shows that the power consumption technology trend (using TTL 5400 component series and GaAs Gate array as a reference) is steadily decreasing. A list of key power supply technology trends and requirement changes affecting the design of supplies and their application in system or equipment designs is presented below.

- Increased power density
- Increased switching speeds
- Increased efficiency
- Increased use of system-distributed power techniques
- Increased use of surface-mounted and hybrid IC technology
- Increased "safe allowable exposed dc voltage" requirements from 42.5V to 60Vdc
- Higher levels of integration in power semiconductors and the advent of economical custom power-control IC's
- Uninterruptible power supplies
- Digitally-controlled power supplies
- Universal input power (operates within the following voltage and frequency ranges: 85 to 264V @ 47 to 440 Hz)

Another key technology trend in equipment design is the use of CMOS and BiCMOS IC technology for reducing power requirements. In conjunction with this trend, system designers are favoring the use of distributed power (dc/dc convertors) more and more to reduce system size and weight requirements. Currently, dc/dc convertors are available with 1 Watt to 500 Watts power ratings which range in size from DIPs to "black boxes". All dc/dc converters are "switches" because switch-mode power supplies are more efficient and smaller than regulated

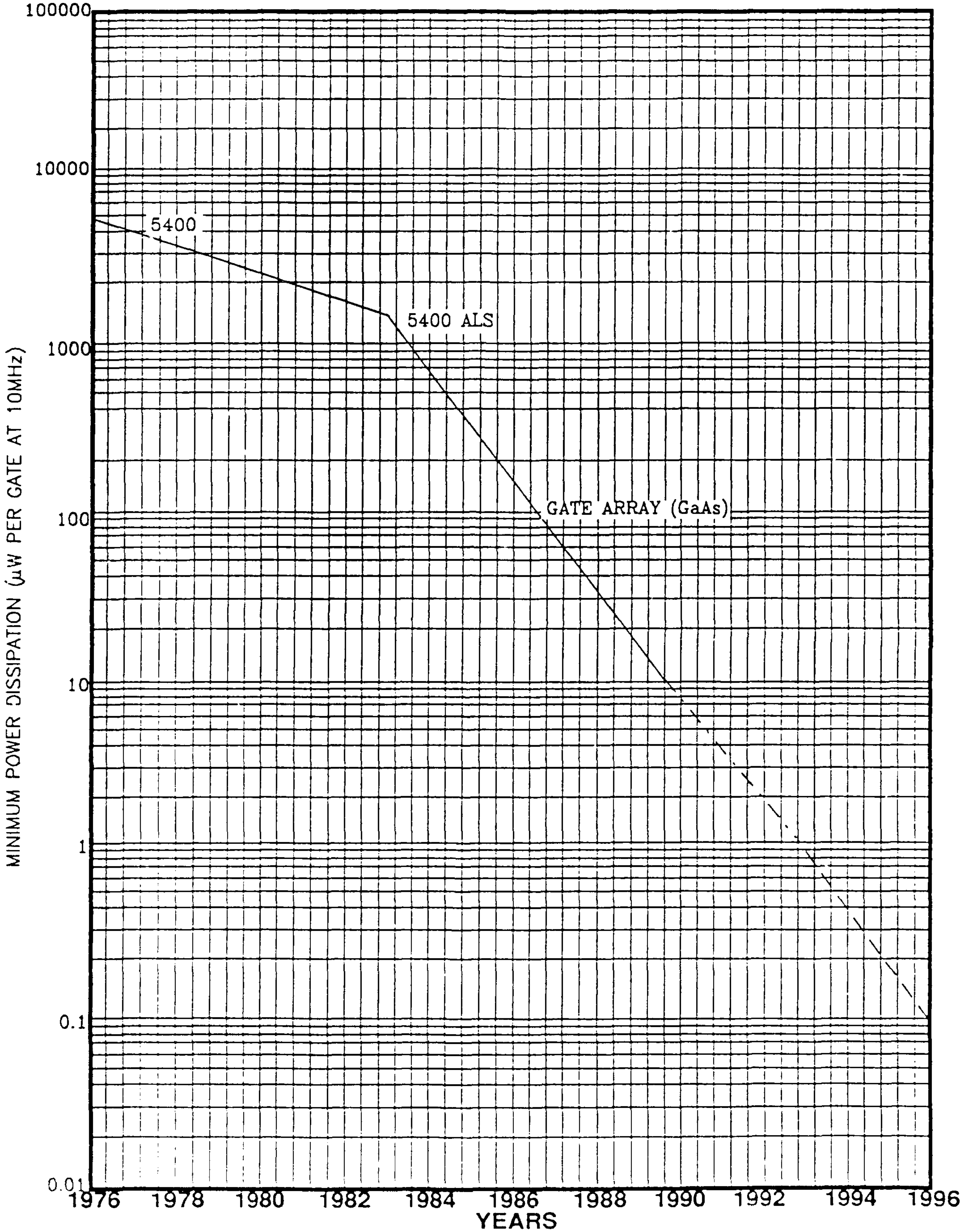

FIGURE 6-1. TREND CURVE FOR IC GATE POWER DISSIPATION

power supplies. Consequently, the switch technology power supplies are rapidly evolving. However, in critical application where tight regulation and low noise are important, the linear regulated power supply is still used and will probably remain for many more years; certainly over six years. Such critical applications that require linear regulated power supplies are:

- Data acquisition circuits
- Automatic test equipment
- Precision laboratory test equipment
- Low-noise amplifiers and signal processing circuits

Likewise, with the research going on in the manufacturing of IC's with geometries less than 0.5 μm, voltage levels required to power IC's will decrease, further reducing future equipment power requirements.

The newest, most dramatic development expected in the power technology world will most likely be the smart power device which will be used for device protection. In the early 1990's, the emergence of these smart power devices is occurring as more energy-conversion building blocks are recast in monolithic silicon. This technology is being driven by the applications integration of traditional analog, power discrete, and digital technologies in a common environment.

Smart power devices are generally made up of two parts: power element and control circuity. The power element can be as simple as using a power-output Field-Effect Transistor (FET) or as complex as working directly with three-phase 220Vac power and then interfacing

to a high current brushless dc motor. The power element's technology goal is to become smart enough to adopt an alternative operating mode when something goes wrong so that only performance is degraded though the system continues to function. Furthermore, it is expected that future smart power devices will also diagnose fault conditions not only in the IC, but also in the system itself.

In addition, according to the National Institute of Standards and Technology (NIST), absolute ac and dc voltage standards will improve in the coming decade. The projected improvements are presented in Figure 6-2 on page 6-6.

6.2.2 INTEGRATED CIRCUITS

Overall, the IC technology is being driven by feature-size downscaling, higher performance in less space, and productivity improvements, while IC products undergo extensive cost-effective growth in performance, density, and reliability. This growth is expected to continue in the next four to six years, and it will bring about increased use of surface-mount devices on PC boards and integration of memory and logic on the same chips, enabling the manufacture of complete analog functional chips that can, through embedded software, perform communications and nonvolatile functions. Furthermore, these future single analog chips are expected to include several integrated communication functions. The underlying developments in standard logic design are faster speeds, lower power consumption (cooler), more cost-efficiency, and greater ease of use. The most popular materials being used to accomplish these goals are GaAs, BiCMOS, and CMOS. GaAs satisfies the ultra-high speed needs, while BiCMOS and CMOS satisfy the high speed, low power, low noise, and high reliability needs which are particularly desirable in military equipment design applications.

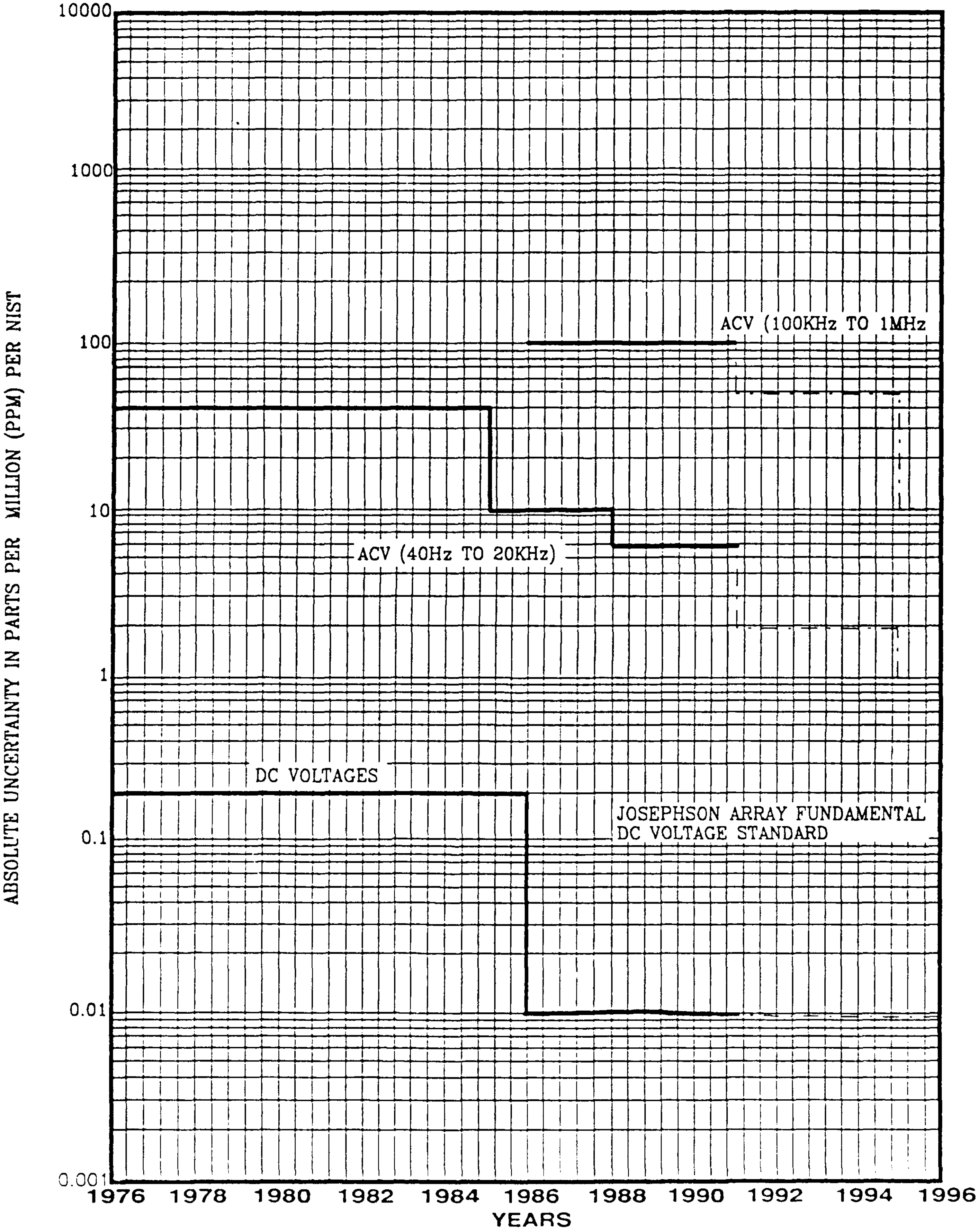

FIGURE 6-2. TREND CURVE FOR ABSOLUTE UNCERTAINTY AC & DC VOLTAGE STANDARDS

ASIC device development is receiving specific attention and is becoming a new kind of commodity logic device, based on ASIC standard-analog cell libraries. Popular versions of ASIC megacells, such as Central Processor Units (CPU's) and programmable logic arrays, will become off-the-shelf items. In four to six years, the increased use of BiCMOS technology and the interweaving of a wide variety of process modules in conjunction with the standard integration process will further drive ASIC density and performance capabilities higher. Production fabrication techniques will enable the manufacture of analog array transistors with cut-off frequencies of 12 to 15 GHz or higher. Also, GaAs will be joining the analog fray, pushing speeds to 80 GHz to make possible real-world analog circuits that can satisfy the digital-signal processing and artificial intelligence needs of the future. These analog arrays are also expected to contain one or more important fixed structures such as a 12-bit digital-to-analog converter or a 8-bit flash analog-to-digital converter for digitization, in addition to repetitive transistor cells. This digitization process is expected to continue for some time, making A/D and D/A convertors an important component (as shown by Figures 6-3 and 6-4, on pages 6-8 and 6-9) resulting in a technology trend towards decreasing bit conversion times and settling times in order to keep pace with faster and faster digital components. These "structured" arrays will maintain their versatility in basic analog circuits while supplying high-performance dedicated blocks.

Next-generation video-processor device designs are integrating peripheral component functions by combining VLSI and digital techniques. Resistance-Inductance-Capacitance (RLC) networks will be replaced by switch-capacitor filters, and A/D converters. All control functions will be accomplished through a general-purpose digital bus, and synchronization circuits will be hybrids, employing both analog and digital technology. The results will be a true mixed-signal device with unique mixed-signal test requirements, as discussed in Section 2.2.2 of Volume 1.

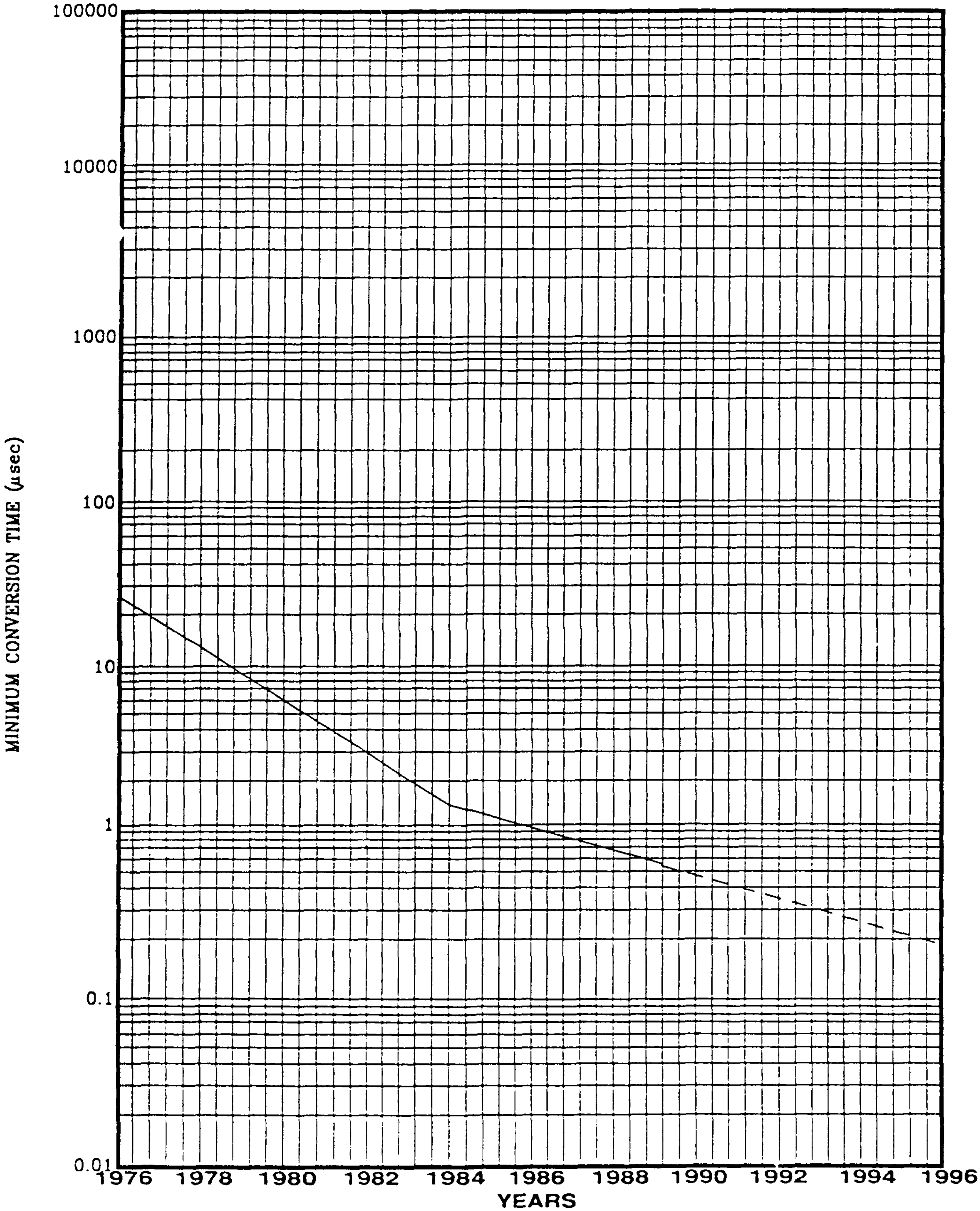

FIGURE 6-3. TREND CURVE FOR 12 BIT A/D CONVERTER CONVERSION TIME

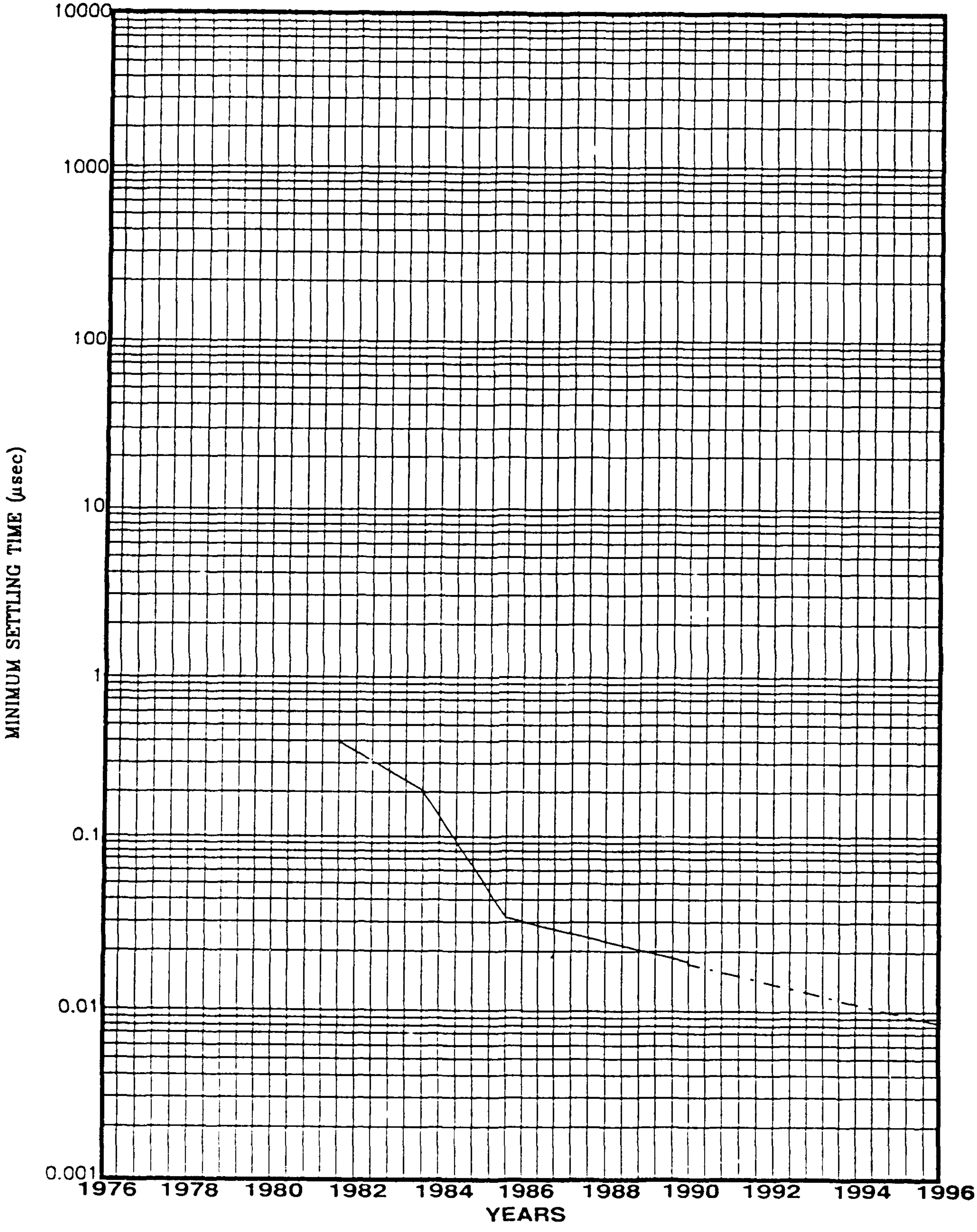

FIGURE 6-4 TREND CURVE FOR 12 BIT D/A CONVERTER SETTLING TIME

Within the next few years, analog arrays or standard cells will increase in number, but they will not dominate the analog world. Operational amplifiers, data converters, and complex hybrid IC's from off-the-shelf will still greatly influence analog design. Analog array architectures will change to accommodate much larger and more diversified array families. Such developments will maximize the efficient use of silicon and increase the types of tasks analog arrays can perform. Also, new processes will be developed continuing the downscaling of IC feature size to achieve nano-electronics. The continuance of this downscaling will most likely be achieved using such technology as quantum tunneling (Reference: Figure 6-5 on page 6-11). The evolution to nano-electronics will also depend upon the use of new materials which are being developed currently in the R&D laboratories. One such candidate for high performance device structures is titanium-silicide which is being used for special communication applications such as propagating microwave and optical signals.

Another key area of industrial research is the reduction of IC geometries to one tenth of the size they are today (less than 0.1 μm). These submicron geometries, together with expanding silicon die sizes and redundant IC design, should make possible Grand Scale Integration (GSI) circuits by the end of the 1990's (Reference: Figure 6-6 on page 6-12).

6.2.3 MONOLITHIC AND MILLIMETER WAVE INTEGRATED CIRCUITS (MIMIC)

In the RF area of technology, MIMIC development is the most significant technology It is regarded as important for the future defense of the United States because of its many military equipment applications. Size and cost reduction, performance assurance, and availability of GaAs MIMIC's are important issues to be resolved for the future of the military system. Some examples of military equipment affected by MIMIC development are listed below.

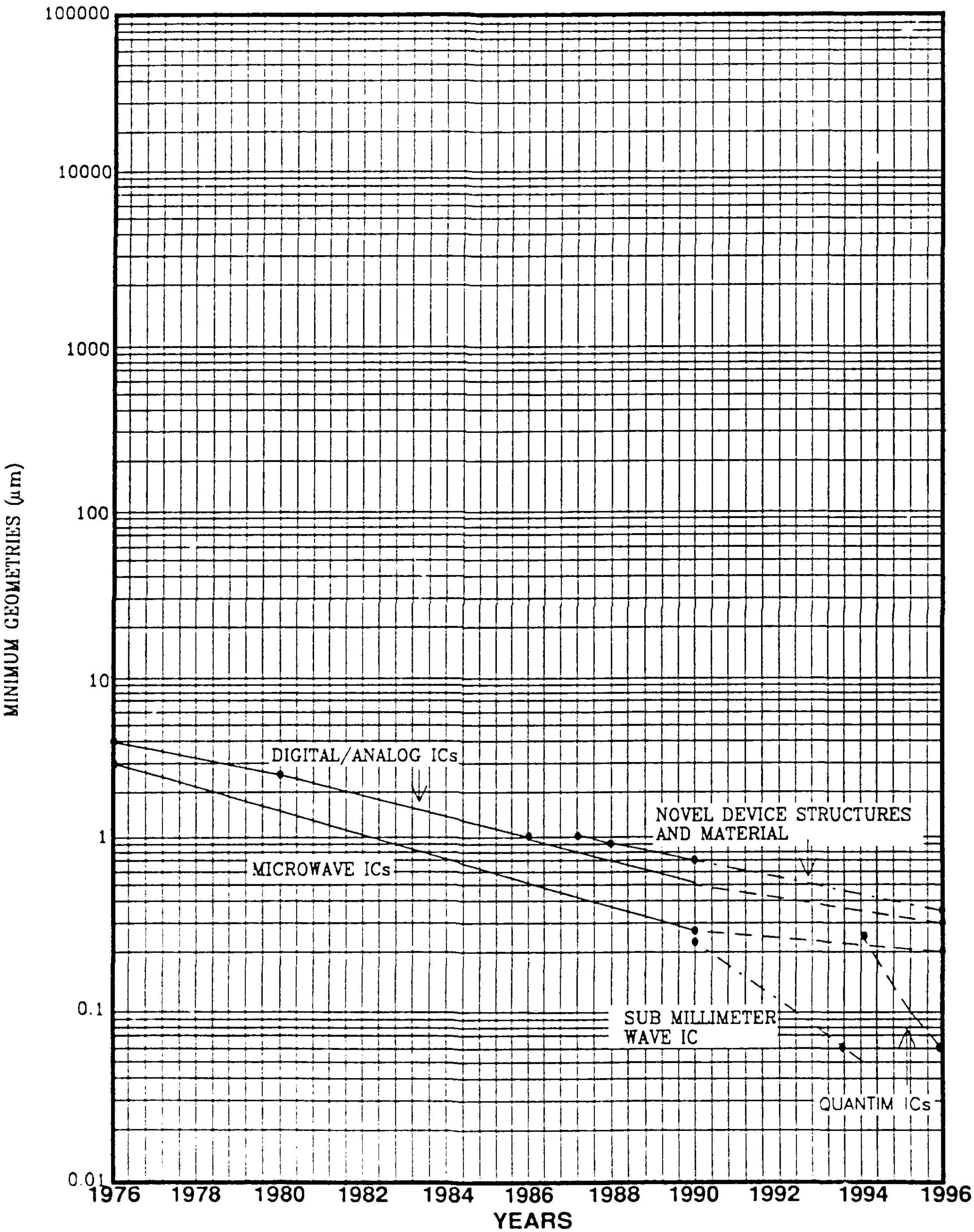

FIGURE 6-5. TREND CURVES FOR MINIMUM IC GEOMETRY

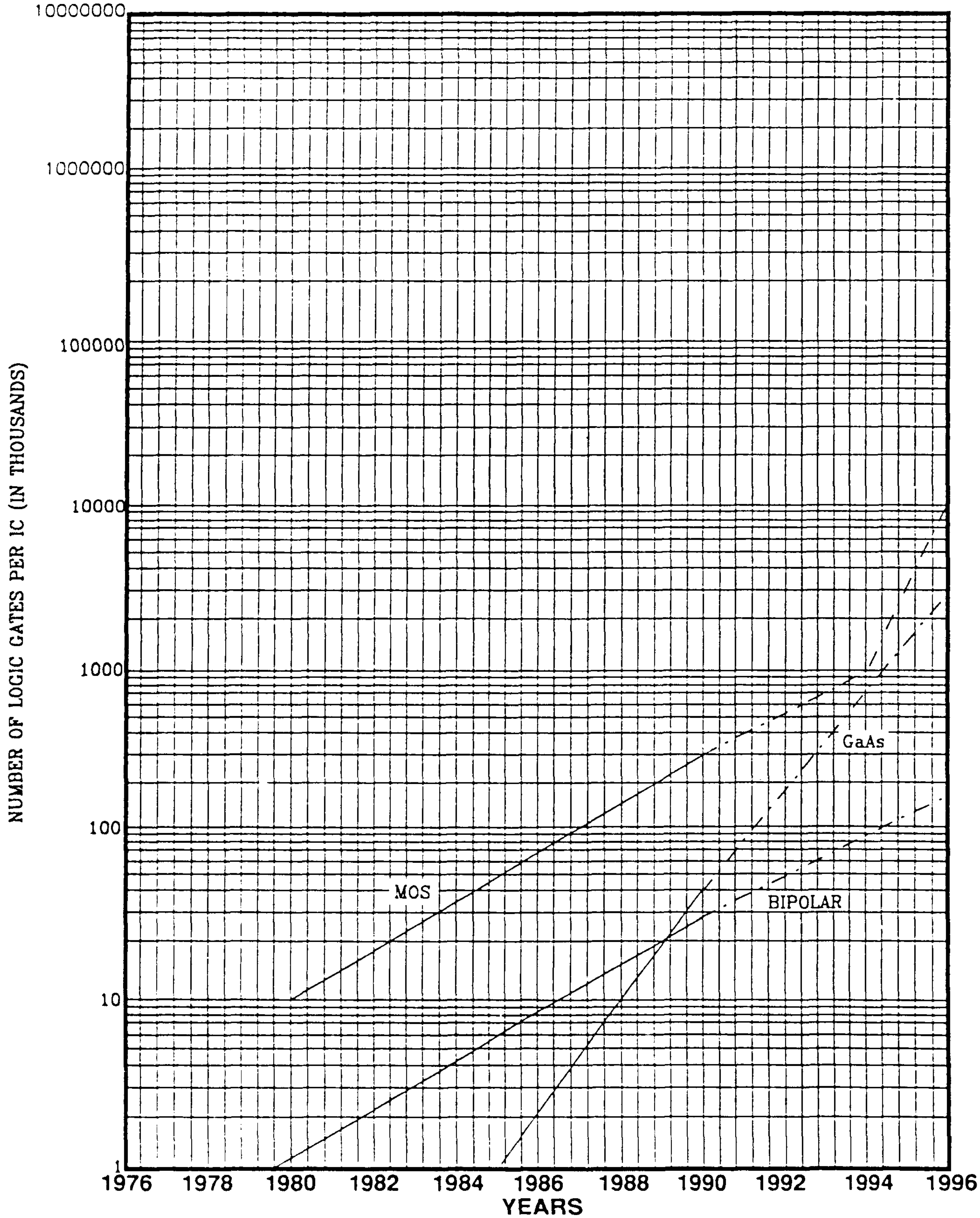

FIGURE 6-6. TREND CURVE FOR NUMBER OF MAXIMUM LOGIC GATES PER IC

- o Transmit/receive array antennas
- o Conformal antennas
- o Frequency agile antennas
- o Antenna control
- o Frequency synthesizer components
- o Transmitters
- o Receivers
- o Seeker/sensor
- o Associated circuits and components

According to military sources, MIMIC technology will be inserted in some procured and fielded systems (e.g., Global Positioning Systems (GPS)) within the next two years, with the aim of improving equipment performance. In other systems (e.g., Missile Launched Rocket System), MIMIC designs are needed to meet both cost and performance requirements. Also, many performance targets of the new phased arrays, smart weapons, and electronic warfare systems will be attainable only through the use of MIMIC technology.

DoD is funding its own R&D program to push the technology threshold into a routine fabrication capability which will satisfy the needs of the military systems. Phase 0 of the MIMIC program, the concept definition stage, was completed in 1988. Phase 1, which is scheduled from May 1988 through May 1991, is developing the following representative chips: five low noise amplifiers operating in the frequency of 1 to 36 GHz, six power amplifiers in the frequency ranges from 5 to 44 GHz, two voltage-controlled oscillators, phase shifters, T/R switches, mixers, attenuators, defectors, and frequency converters. As with analog IC's, MIMIC Phase 1 is also fabricating multi-function chips for economy of production and compactness

of design. For example, a single chip will be capable of performing phase shifting, amplification, and switching.

Commercial MIMIC R&D has a headstart, but it is still in its infancy. Commercial efforts in the laboratory have produced MIMIC components. For example, the following MIMIC components have been announced:

- 1-18 GHz 35 dB Gain Amplifier (Thompson-CSF)
- 2 GHz Oscillator (Motorola)
- 40 GHz Control Circuit (Alpha Industries)

It appears that the major MIMIC product R&D efforts are being expended in the 1 to 110 GHz frequency range, and the main semiconductor material being used is GaAs.

6.2.3.1 RF SYSTEM ATTRIBUTE PROJECTIONS

Because of the advent of MIMIC and VHSIC technology, the general RF system attributes described below should make achievable, within the next four to six years, the technology projections presented in figures 6-7 through 6-14.

6.2.3.1.1 OPERATING FREQUENCY (Reference: Figure 6-7 on page 6-15)

The move to higher and higher operating frequencies is being driven by the DoD funding of such programs as VHSIC and MIMIC. It is expected, based upon the data collected, that such funding programs will produce electronic equipment (e.g., fixed-frequency antennas

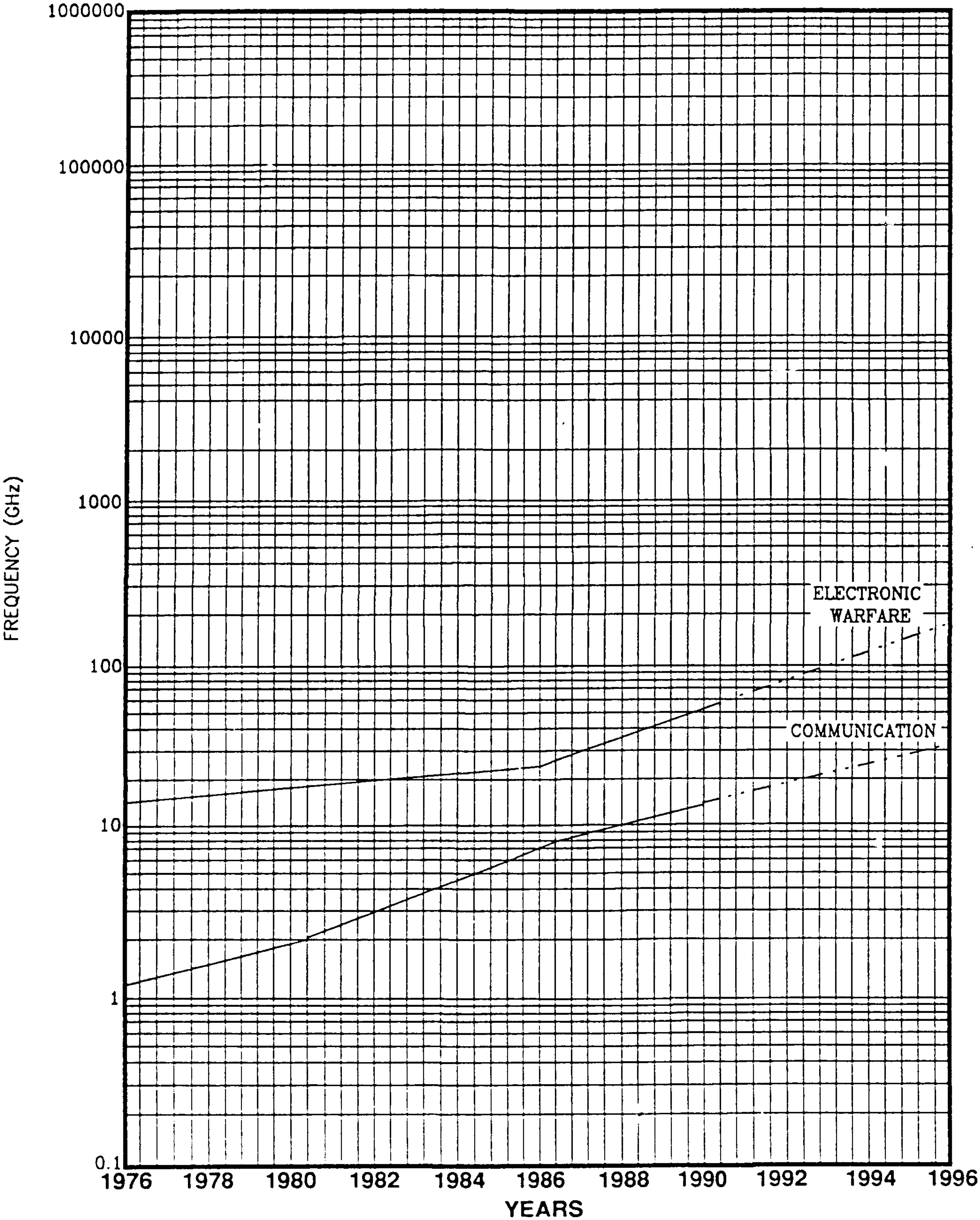

FIGURE 6-7. TREND CURVE FOR MAXIMUM RF OPERATING FREQUENCY

and solid-state distributed amplifiers) that operate in the 94 GHz to 110 GHz frequency range. Beyond six years, it is expected that high-power lasers will replace millimeter wave oscillators in satellite, accounting for some very high frequency projections for RF systems in the next century.

6.2.3.1.2 SOLID-STATE DEVICE CONTINUOUS WAVE OUTPUT (Reference: Figure 6-8 on page 6-17)

With the continuing DoD funding of the MIMIC program, the ability to produce higher power solid-state continuous wave output devices is expected to be greatly enhanced. Some specific developments in this area are a 94 GHz planar chip, a Cryo-cooled distributed travelling continuous wave (CW) transmitter, and the use of more efficient material for Impact Avalanche Transit Time (IMPATT) devices. Currently, solid-state devices of these types have the capability of outputting around 3 Watts. However, with improved cooling (e.g., diamond substrate, heat pipes) this capability is expected to increase to 10 Watts for a single device in four to six years. Another approach to generating higher power is the design of arrays that effectively permit a number of devices to work in concert to produce higher power levels, possibly reaching 30 Watts and up to 60 GHz by the end of this decade.

6.2.3.1.3 BANDWIDTH (Reference: Figure 6-9 on page 6-18)

To increase bandwidth, present circuit techniques will have to be improved. One approach is to use planar techniques. However, it is expected that the bandwidth will not exceed fifty percent of the operating frequency because fundamental physical limits, such as limits on antennae couplers, are reached at that level.

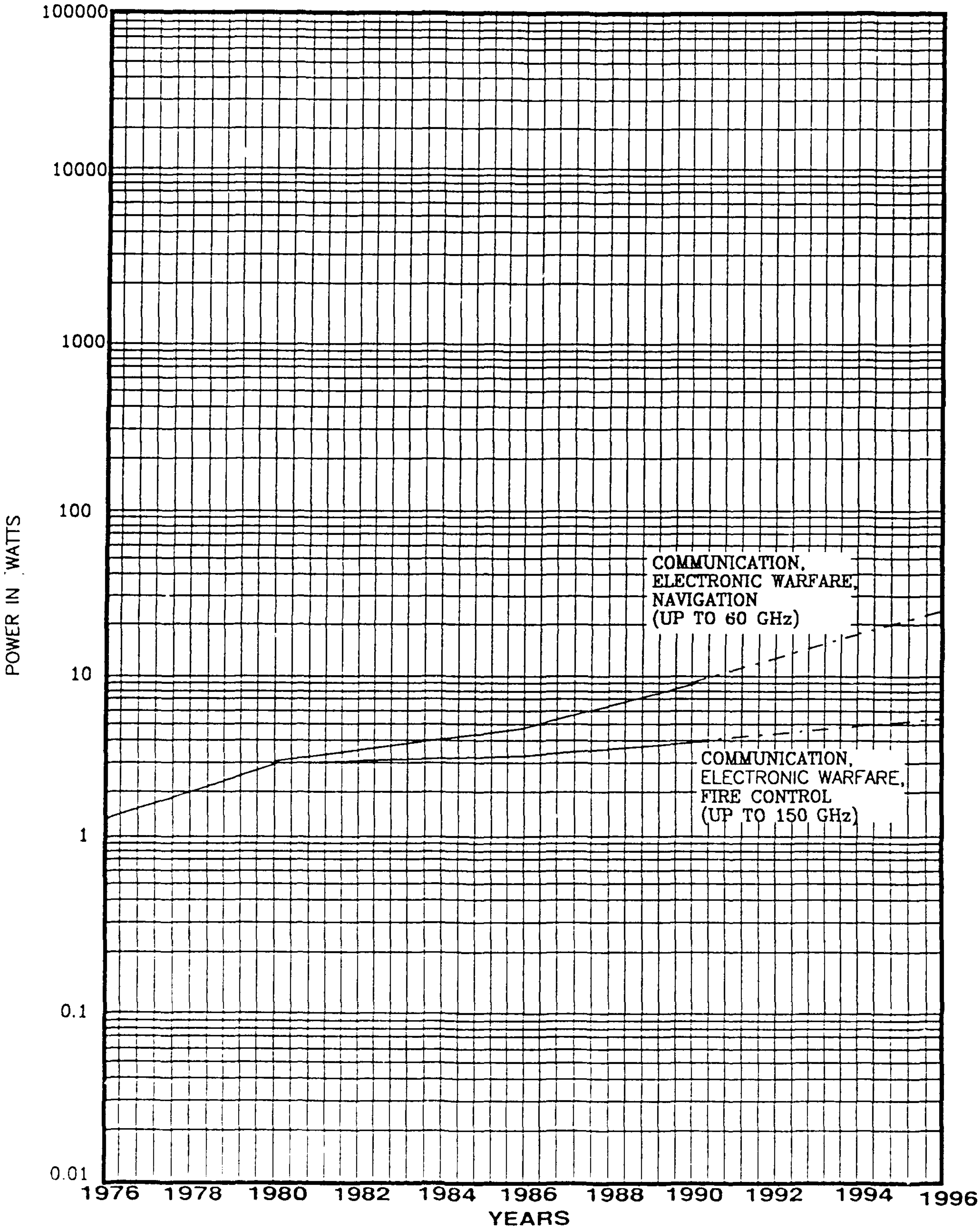

FIGURE 6-8. TREND CURVE FOR SOLID-STATE DEVICE MAXIMUM CONTINUOUS RF WAVE OUTPUT

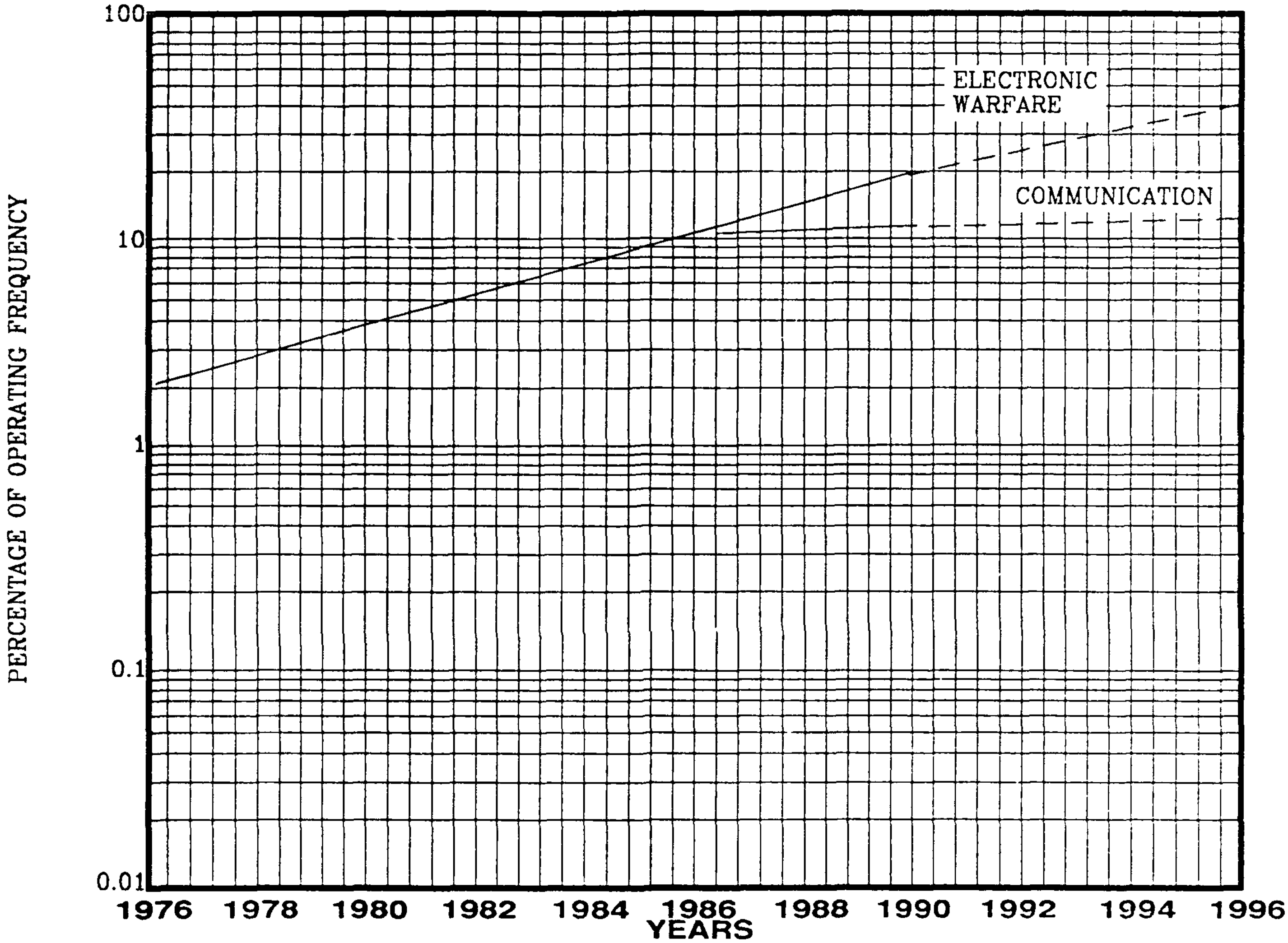

FIGURE 6-9. TREND CURVE FOR MAXIMUM RF BANDWIDTH

6.2.3.1.4 **OUTPUT POWER** (Reference: Figure 6-10 on page 6-20)

The technology trend driver for increased output power development will be electronic warfare systems design requirements. The expected increase in output power is by one order of magnitude over current output power capabilities due by the end of the decade. This increase will be brought about by improvements in the design of Travelling Wave Tube (TWT) amplifiers along with improved TWT system power supply designs and power conversion efficiency.

6.2.3.2 SPREAD SPECTRUM ATTRIBUTE PROJECTIONS

MIMIC and VHSIC will drive the spread spectrum technology. According to the survey, spread spectrum technology is seeking improvement in frequency synthesizer performance, frequency phase agility, system bandwidth, equipment size, component power consumption, filtering design and high speed logic. The key performance attribute projections for spread spectrum technology are listed below.

6.2.3.2.1 **FREQUENCY/PHASE AGILITY** (Reference: Figure 6-11 on page 6-21)

The survey consensus was that the increase in the agility of frequency/phase changes in spread spectrum systems will depend greatly upon the availability of MIMIC and VHSIC designs for fast-switching digital synthesizers and other technology development such as low-cost digital correlators, Surface Acoustic Wave (SAW) resonators, comb filters for frequency synthesizers, smart synthesizers with very fast settling times to reach higher frequency rates, and GaAs RF elements. Also, greater security for communication systems is expected to push transmitting frequency levels continually higher into the range over 200 GHz, as depicted in

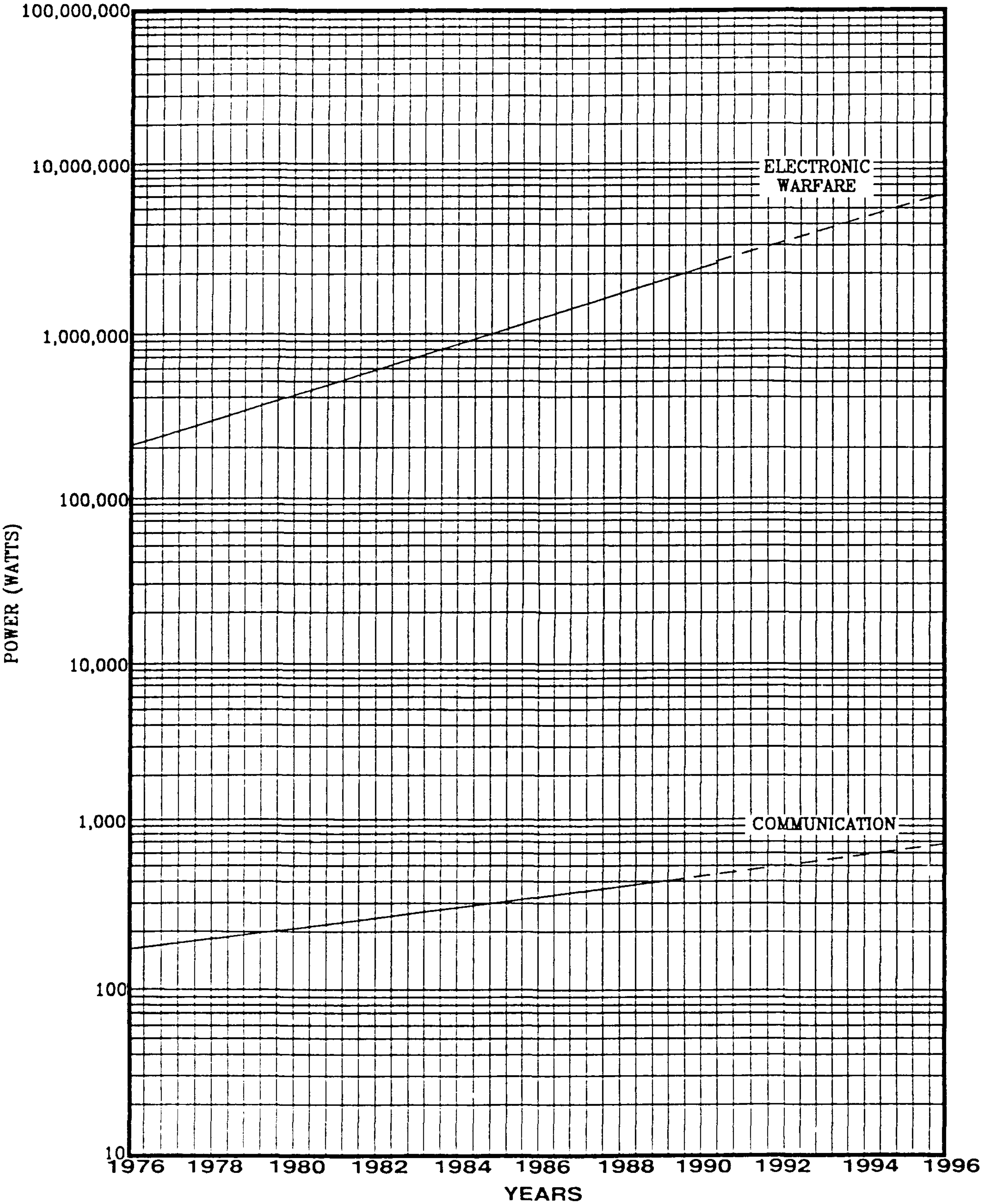

FIGURE 6-10. TREND CURVE FOR MAXIMUM RF OUTPUT POWER

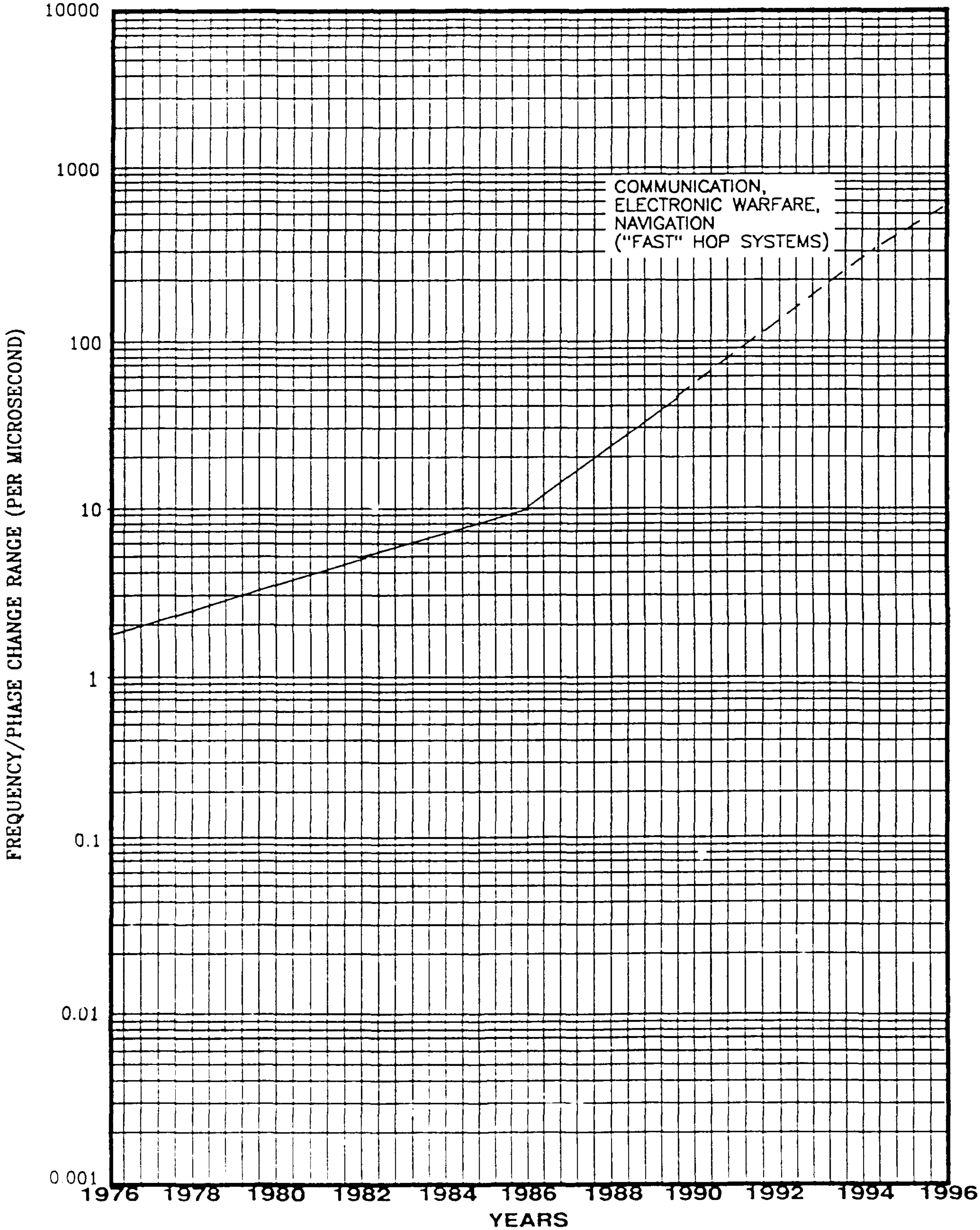

FIGURE 6-11. TREND CURVE FOR GREATEST RF SPREAD SPECTRUM FREQUENCY/PHASE AGILITY

Figure 6-11, with frequency/phase change rates of 1 billion per second by the end of this decade.

6.2.3.2.2 MAXIMUM BANDWIDTH (Reference: Figure 6-12 on page 6-23)

The maximum bandwidth is expected to increase due to the employment of the following technologies in the spread spectrum system: integrated optical-electronics, wideband frequency synthesizers, advanced digital circuits, and higher millimeter wave frequencies using MIMIC technology.

Based upon the technical survey, spread spectrum system bandwidths are expected to increase the use of MIMIC technology currently developed. Frequency hopping is expected to reach one billion transitions per second at a center frequency of 250 GHz with system bandwidths of 225 GHz to provide greater security in communications.

6.2.3.2.3 SYNCHRONIZATION TIME (Reference: Figure 6-13 on page 6-24)

Survey data indicates that the degree of synchronization time improvements will depend upon specific developments that are expected to include: SAW matched filters for parallel processing of VHSIC matched filters and VHSIC Coders/Decoders. If VHSIC chips with parallel channels for processing are achieved in the near future, synchronization times are expected to go below 0.1 nanoseconds by the end of the decade.

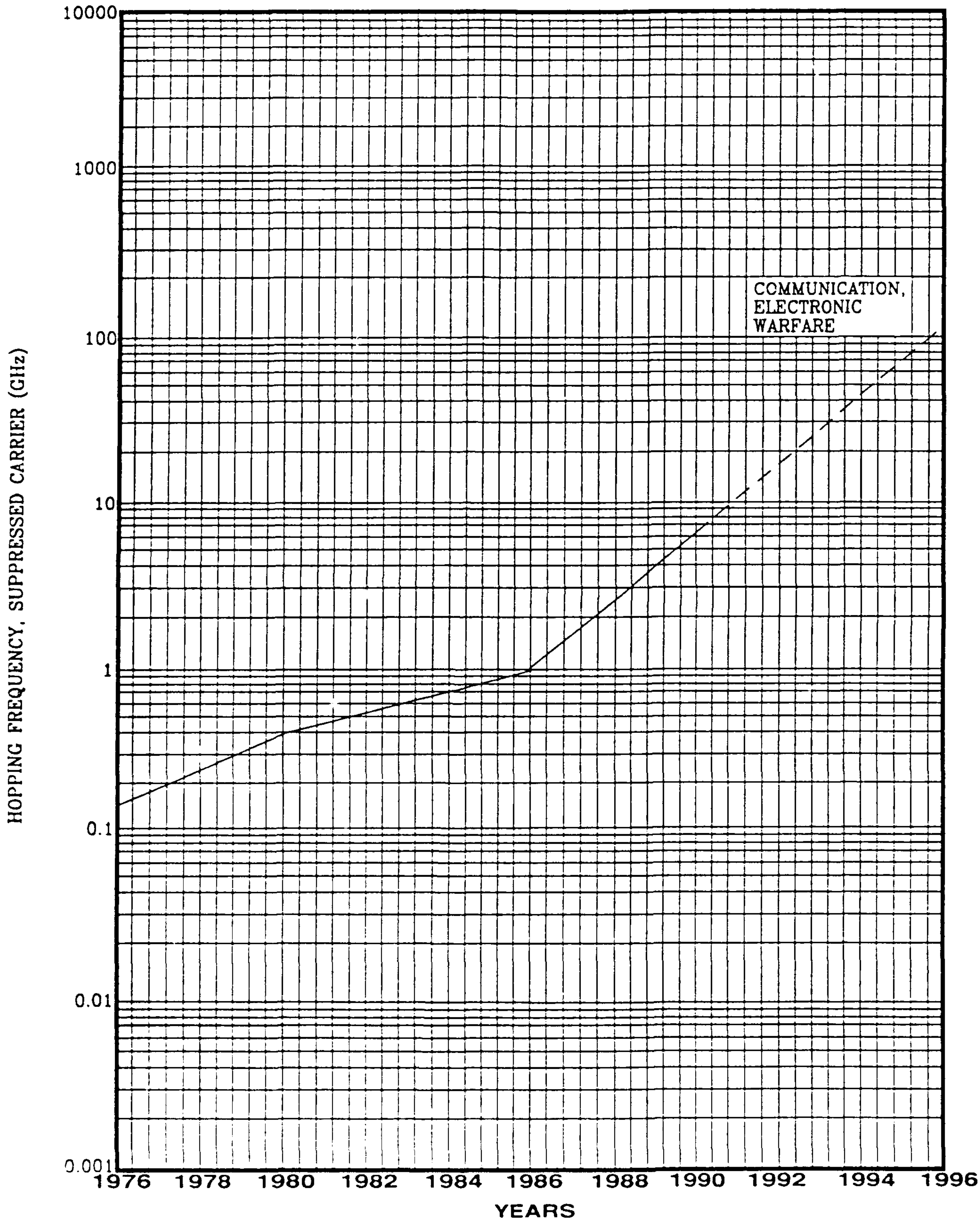

FIGURE 6-12. TREND CURVE FOR RF SPREAD SPECTRUM MAXIMUM BANDWIDTH

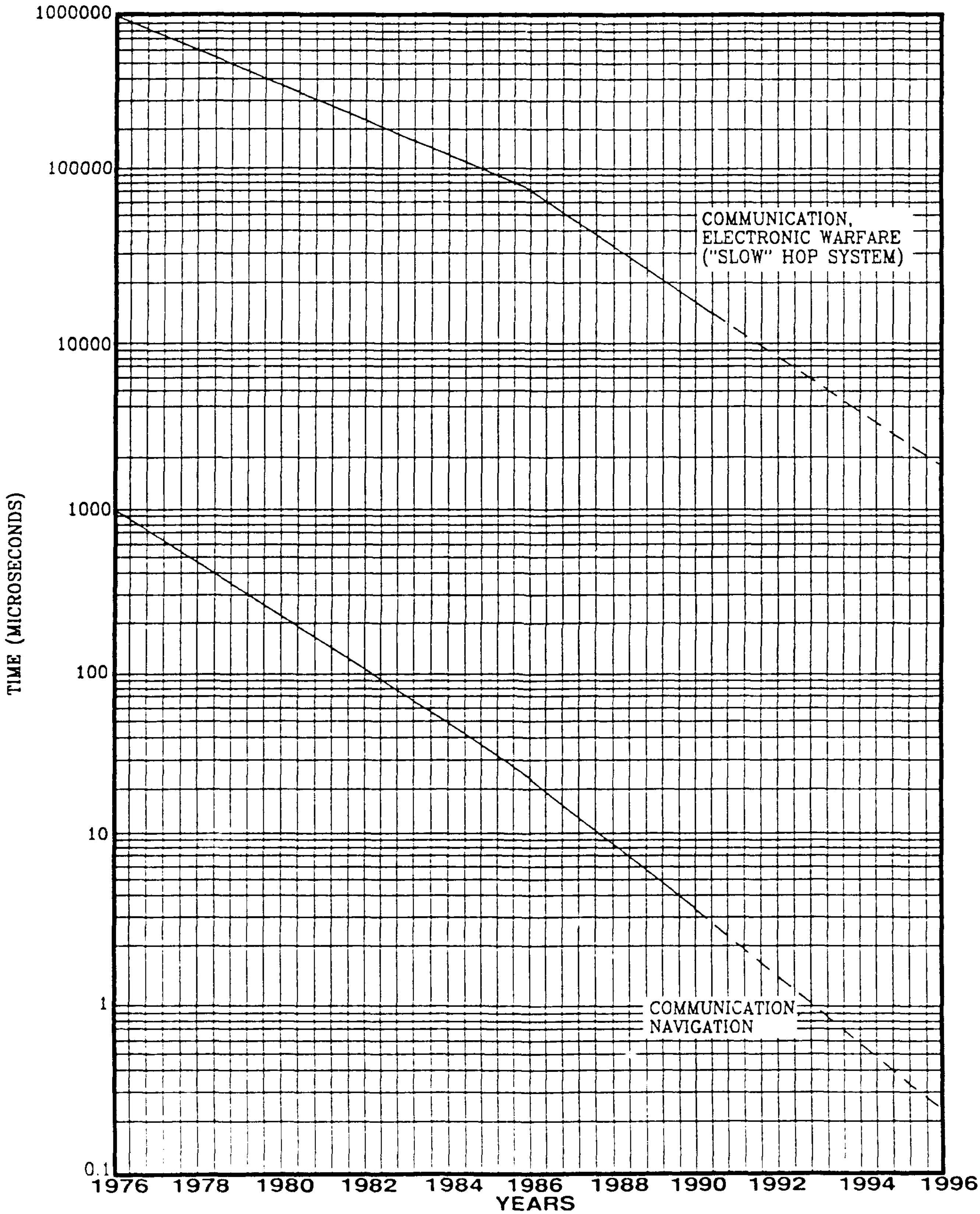

FIGURE 6-13. TREND CURVE FOR RF SPREAD SPECTRUM MAXIMUM SYNCHRONIZATION TIME

6.2.3.2.4 TRANSMITTER POWER OF ANTI-JAMMING SYSTEMS (Reference· Figure 5-14 on page 6-26)

The survey indicates that solid-state anti-jamming system technology will be improved by development efforts in solid-state microwave power, adaptive side-lobe emitters, array combers and multiple-element emitters. The radiated power of solid-state silicon IMPATT is expected to reach approximately 10 Watts by the end of the decade; however, the real high power systems will use travelling wave tubes. The trend curve projects the travelling wave tube technology since other high-power technology is not currently comparable in power levels.

6.2.4 SYNCHRO/RESOLVER

Based upon the data collected, Synchro/Resolver technological improvements will most likely be in the area of downsizing of Synchro/Resolver circuitry through the use of custom IC's, tracking rates, greater degree accuracies, and resolution performance of Synchro/Resolver IC's. Unfortunately, data regarding the magnitude of these improvements was not sufficiently conclusive to produce a technology trend.

6.3 OPTICAL

Because military application of fiber optics technology is just beginning, the military data on this technology is limited. Commercial optical technology data had to be used to make any technology forecasts. Presently, fiber optic utility for data handling in military systems is perceived by the cognizant planners as very promising. Therefore, technology insertion of fiber optics is occurring on such existing aircraft as the F-15 and will certainly continue to be

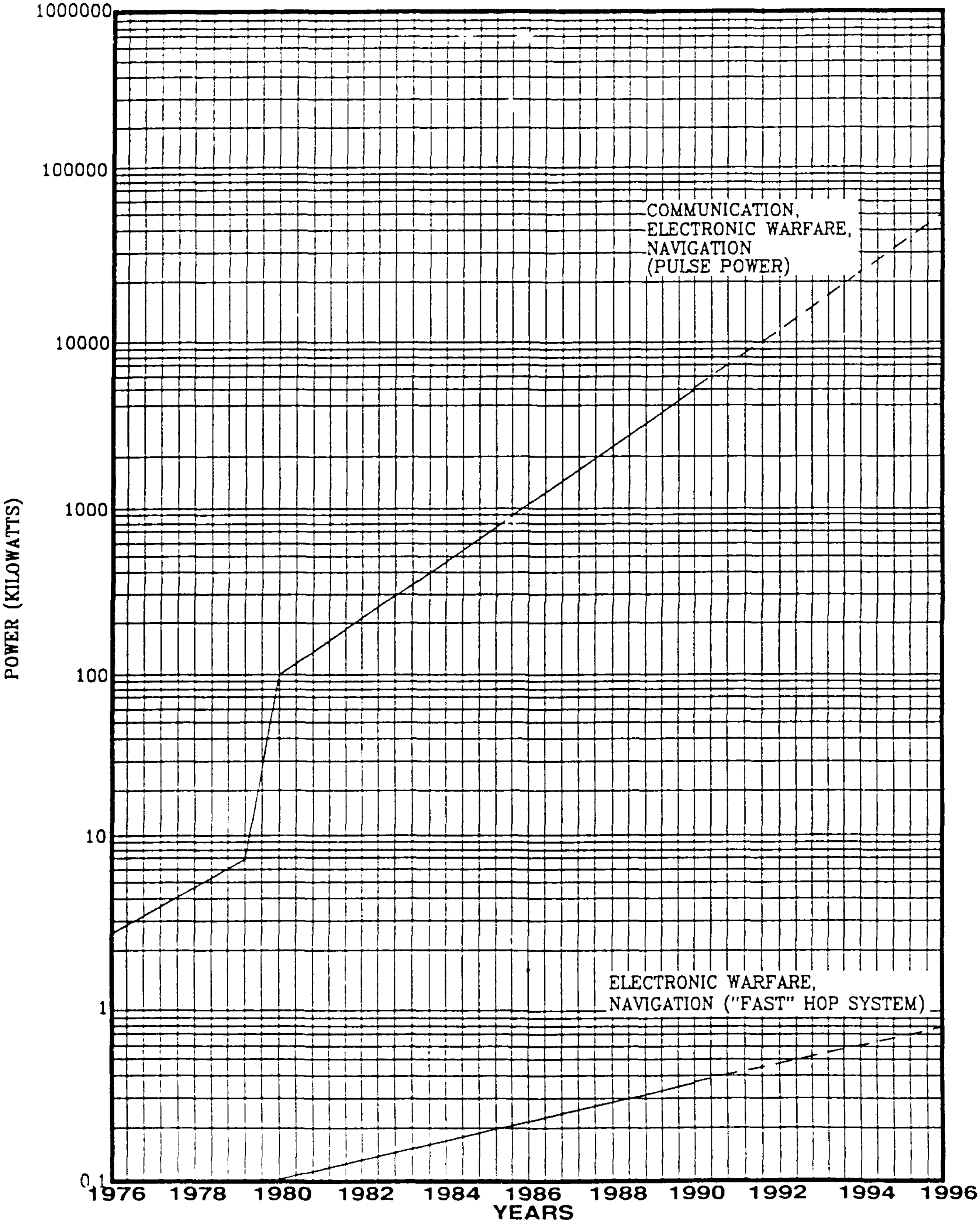

FIGURE 6-14. TREND CURVE FOR RF SPREAD SPECTRUM MAXIMUM TRANSMITTING POWER OF ANTI-JAMMING SYSTEM

used on new aircraft. This technology will provide aircraft with bus data rate of 50 Mb/s and higher in the future, as compared to metal cable rates of 1 through 10 Mb/s. Some key optical system technology attributes are forecasted below:

6.3.1 NETWORK SIZE (Reference: Figure 6-15 on page 6-28)

Growth in network size will be dependent upon the development of low-loss couplers suitable for military systems. Currently, optical couplers are a major problem in fiber optic systems because of their high losses and the variability of these losses. Fundamentally, the network size is predicated on the basic military communication requirements. The survey indicates that for the next four years, a network of 32 to 216 nodes should be sufficient for 90% of the applications.

6.3.2 NETWORK CAPACITY (Reference: Figure 6-16 on page 6-29)

Network capacity will be driven by mission requirements. These requirements include the application of new technology, development of new mission sensors, and the development of fiber optic communication systems within Air Force electronic systems. The survey consensus is that fiber optic wave multiplex systems are needed to handle growth in capacity.

6.3.3 DATA RATE (Reference: Figure 6-17 on page 6-30)

The amount that data rates will increase in the future depends upon the development of improved couplers with better part-to-part uniformity and lower insertion loss, and the development of materials that allow high bandwidth integrated electro-optics to be used.

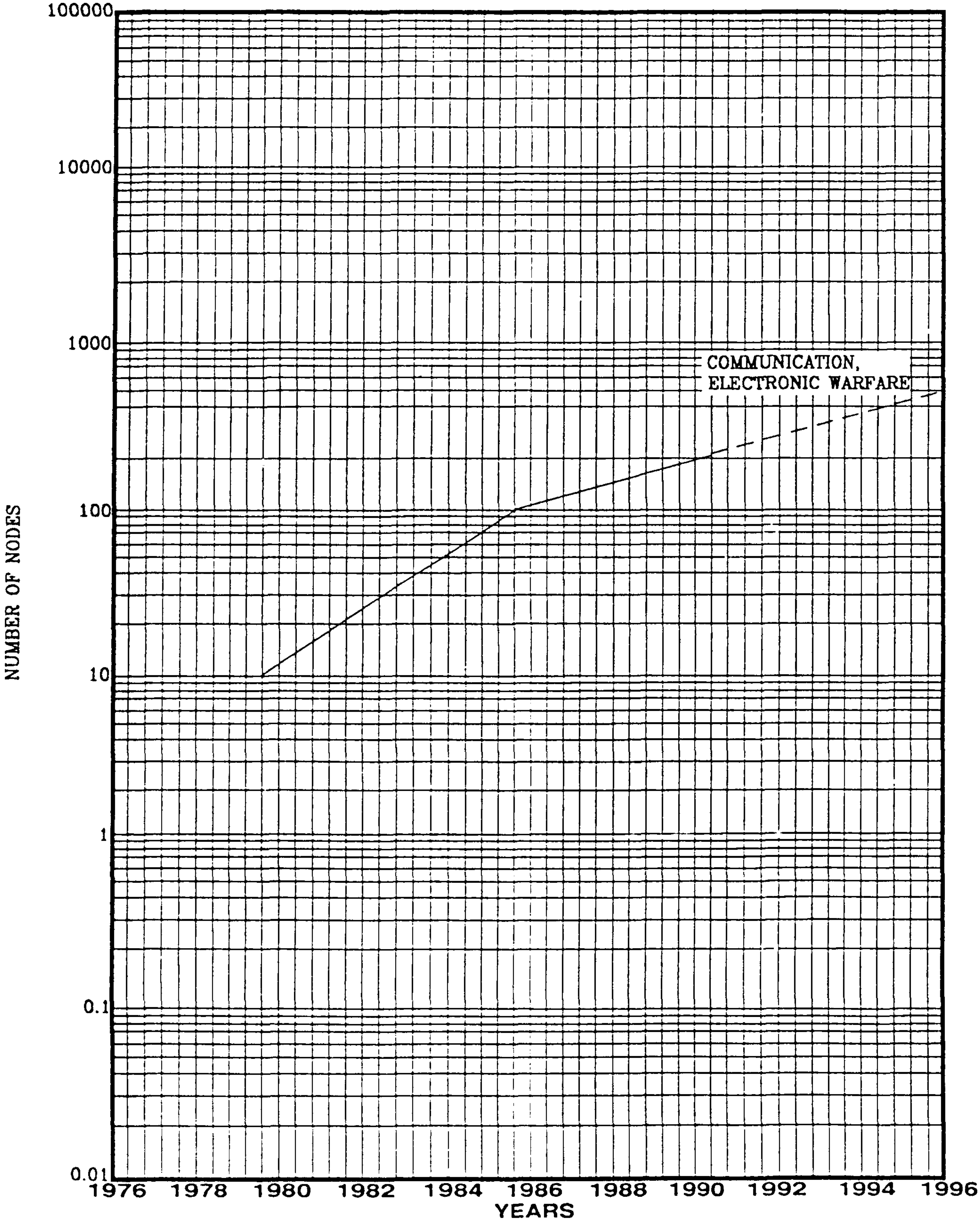

FIGURE 6-15. TREND CURVE FOR OPTICAL SYSTEM MAXIMUM NETWORK SIZE

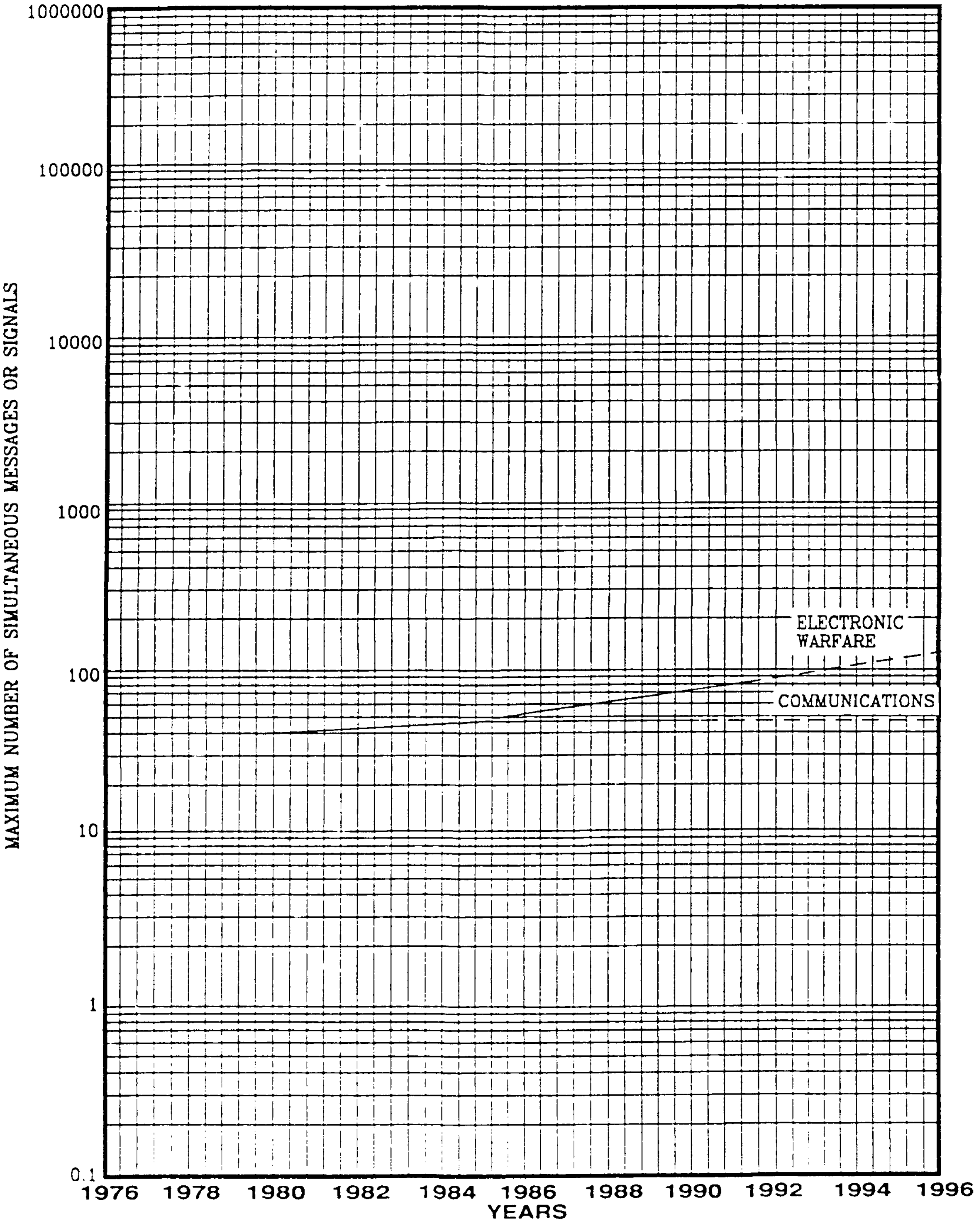

FIGURE 6-16. TREND CURVE FOR OPTICAL SYSTEM NETWORK CAPACITY

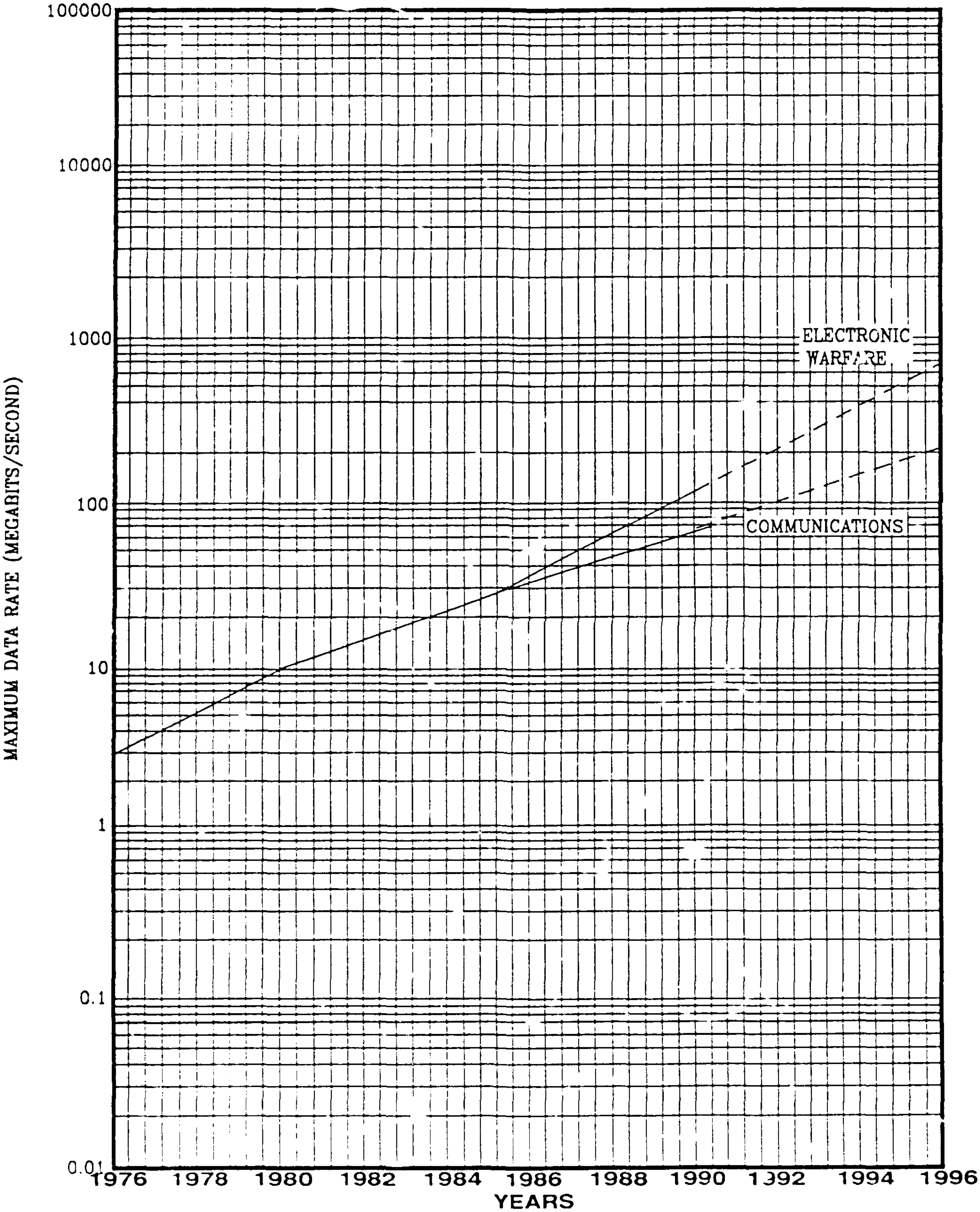

FIGURE 6-17. TREND CURVE FOR OPTICAL SYSTEM DATA RATE

Currently, fiber optic technology permits approximately 400 megabits per second transmissions. Data rates in certain applications are expected to increase to 1 gigabits per second by the end of this decade.

6.3.4 COUPLER LOSS VARIABILITY (Reference: Figure 6-18 on page 6-32)

The desire for lower coupler loss variability results from the fact that such variability places major design and system constraints on fiber optic transmitters and receivers. It is expected that in the coming years, improved optical connectors, the development of high quality fibers, and R&D initiatives in the commercial marketplace will result in low coupler loss variability.

6.3.5 RECEIVER SENSITIVITY AND TRANSMITTER POWER (Reference: Figure 6-19 and 6-20 on page 6-33 and 6-34, respectively)

Receiver sensitivity and transmitter power together with coupler losses are important co-variables which must be addressed for fiber optic system maintenance support. Improvement must be made to significantly increase network size in the future.

6.3.6 OPTICAL DISK (Reference: Figure 6-21 on page 6-35 for Data Storage Capacity and Reference: Figure 6-22 on page 6-36 for Data Transfer Rate)

The technology trends regarding optical disks are the increased use of erasable optical storage disks instead of read only and write once optical storage disks; increased storage capacity from hundreds (typically 640 Mbytes) of megabytes to thousands (forecasted to be 6000 to 7000 Mbytes in the next four to six years) of megabytes on a 5.25-inch disk; and

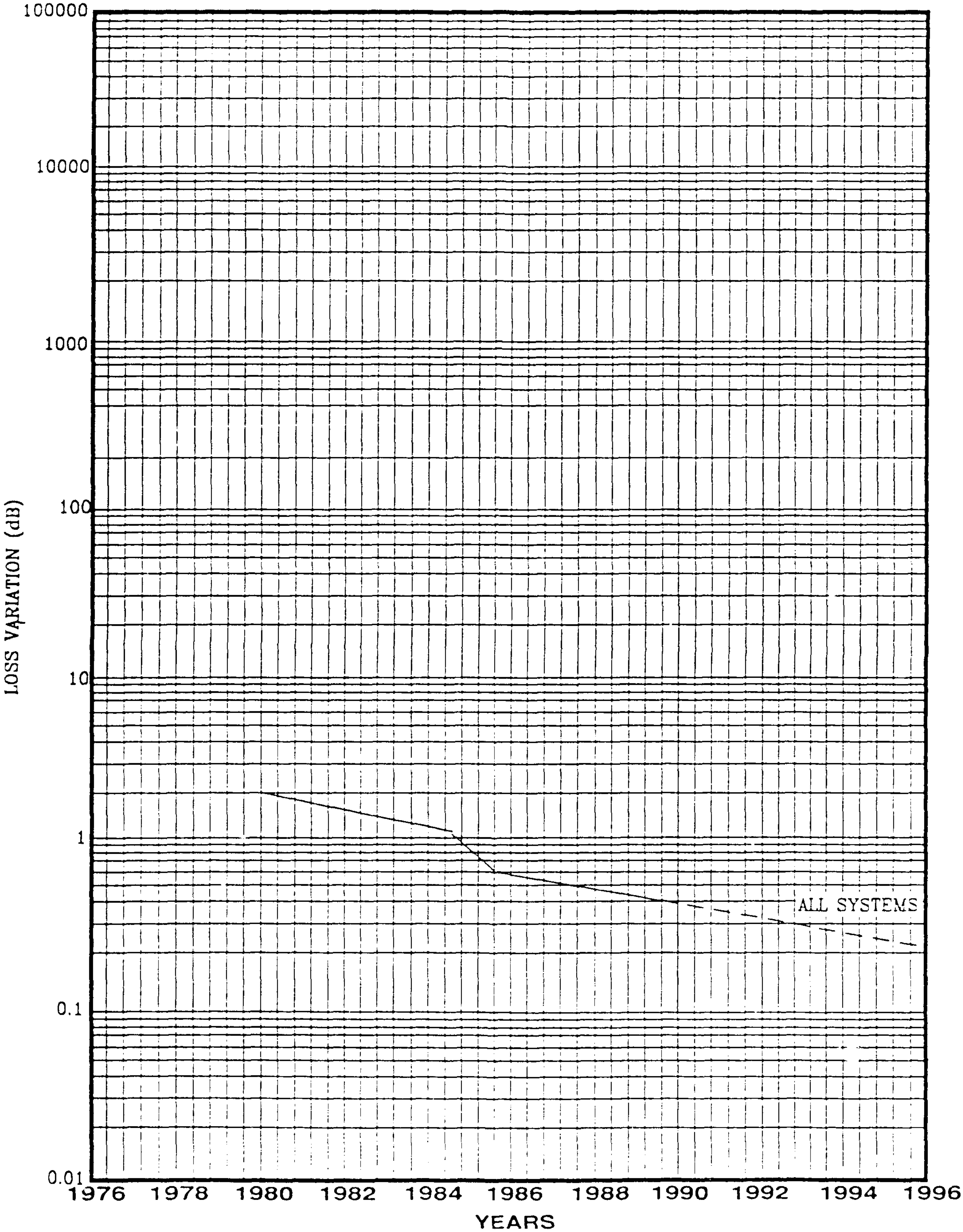

FIGURE 6-18. TREND CURVE FOR OPTICAL FIBER COUPLER AVERAGE LOSS VARIATION

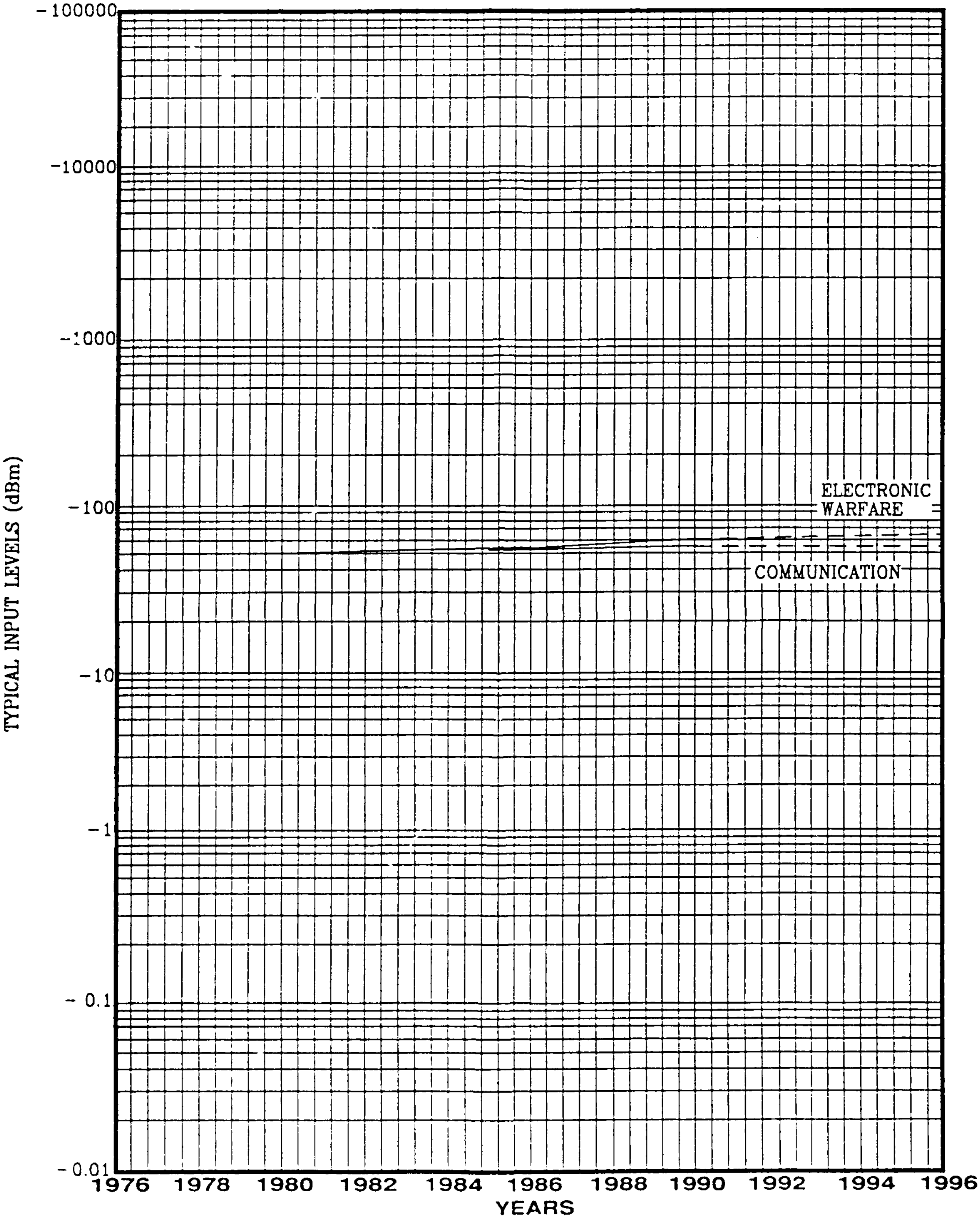

FIGURE 6-19. TREND CURVE FOR OPTICAL SYSTEM RECEIVER SENSITIVITY

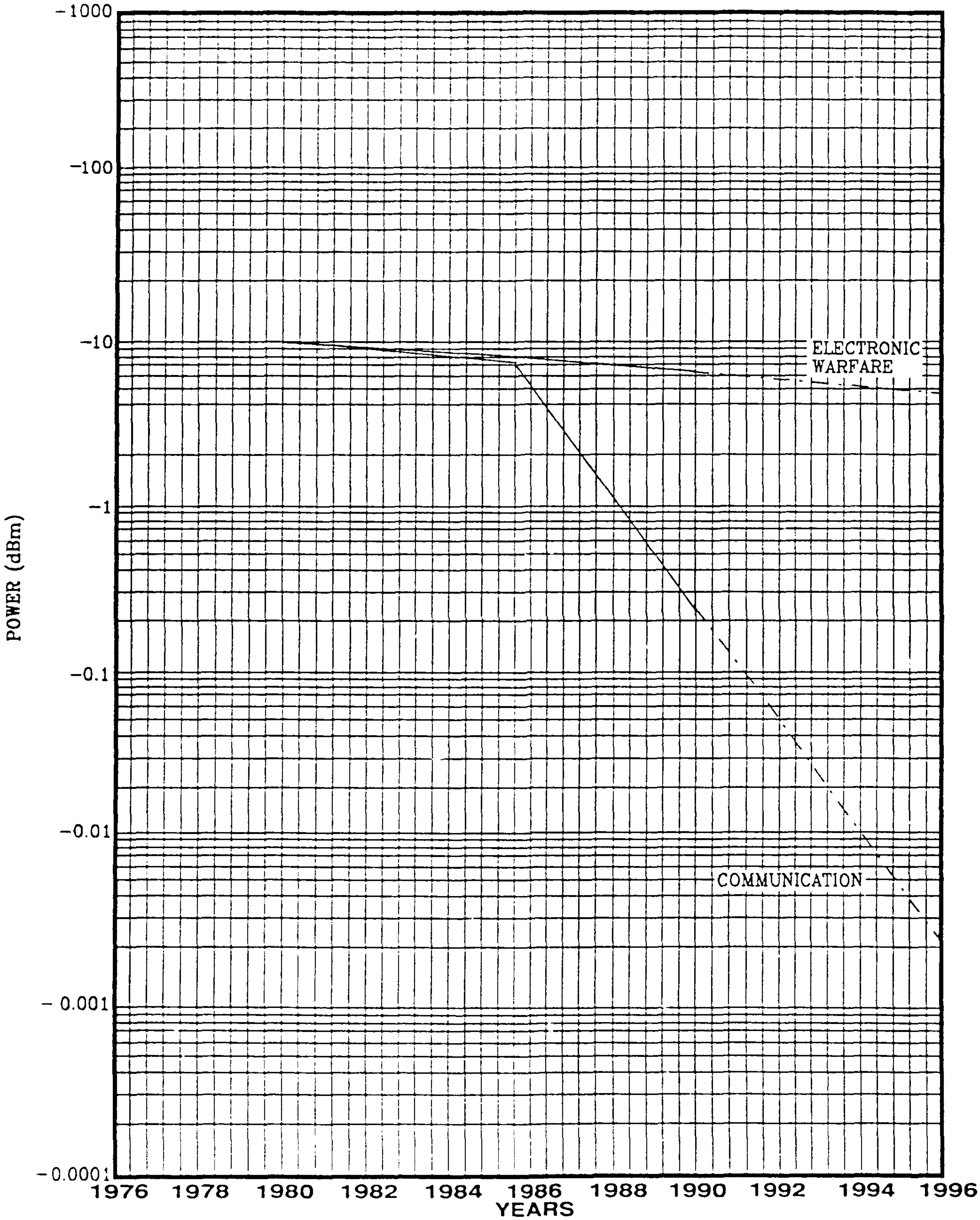

FIGURE 6-20. TREND CURVE FOR MAXIMUM OPTICAL TRANSMITTER POWER

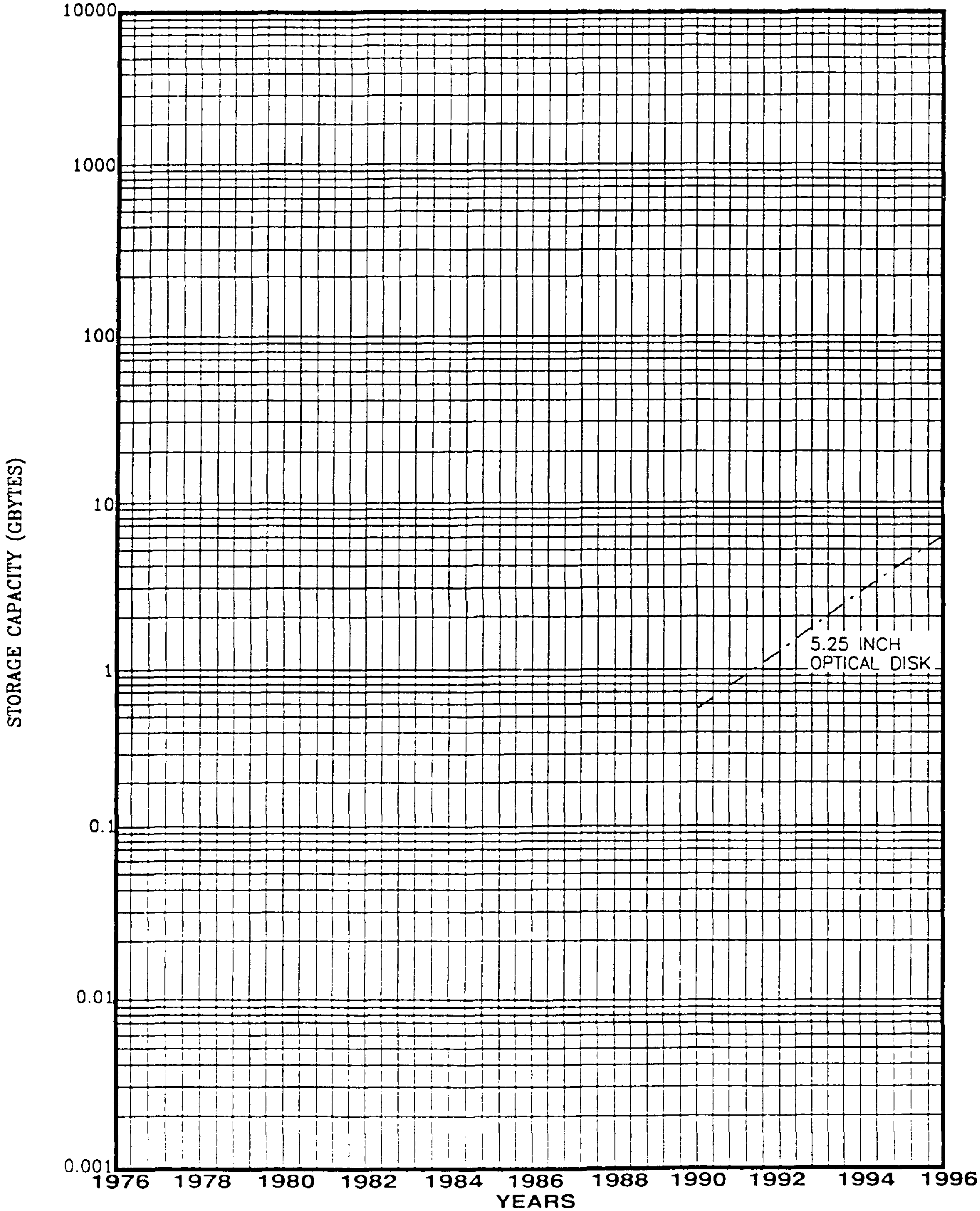

FIGURE 6-21. TREND CURVE FOR OPTICAL DISK TYPICAL STORAGE CAPACITY

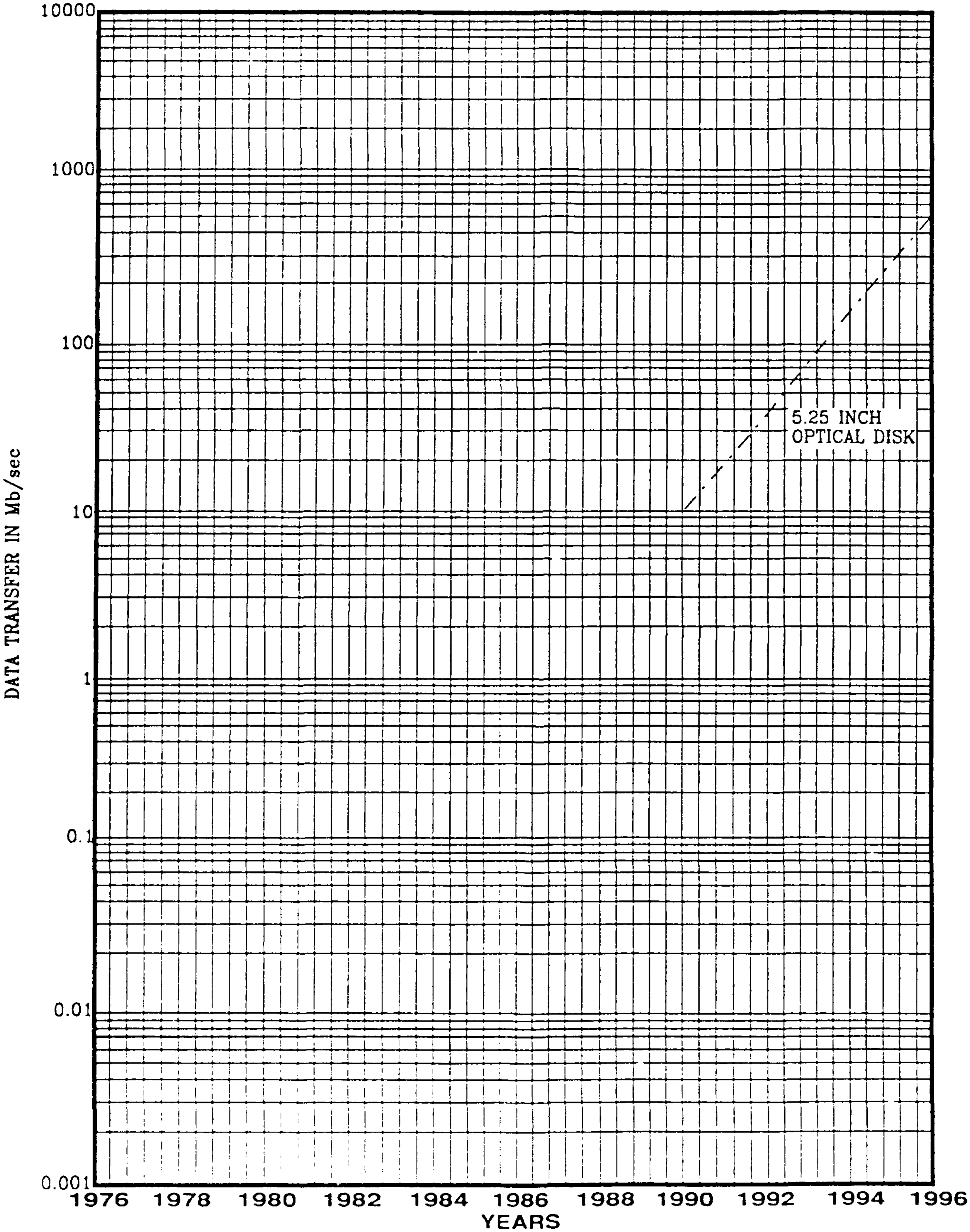

FIGURE 6-22. TREND CURVE FOR OPTICAL DISK DATA MAXIMUM TRANSFER RATE

increased data transfer rates from 1 megabit (typically 10Mb/s) to hundreds of megabits per second (forecasted to be 500 Mb/s in the next four to six years).

One of the most significant technological trends to develop recently is the onset of an optical fiber capable of providing high bandwidth and low attenuation, with the use of single mode fiber versus multimode fiber.

Besides fiber optics, there seems to be a consensus among manufacturers that use of integrated optics is another trend of the future. Devices that combine or integrate emitters, detectors, couplers, and connectors will become an increasingly attractive and inexpensive alternative to the present components. Integrated optics will increase system performance since the packaging will be factory assembled and, therefore, less prone to error. An example of such integrated optics devices involves the use of optical signals to provide high-speed control of solid-state microwave devices at high power levels. This has attracted the attention of many developers.

Fiber-optics technology offers the following advantages:

- High resistance to electromagnetic interferences
- Downsizing and weight reduction through replacing waveguide and heavy metal cable with lighter weight fiber optics cables
- Perfect isolation between the microwave circuit and the input control signal

Several techniques exist for accomplishing this microwave signal control by an optical signal. These techniques include: opto-electronic switching of microwave in silicon using GaAs technology to generate short bursts of microwave signals with complex waveform and optical

switching of GaAs IMPATT oscillator. The type of optical signal to use depends upon the application. Listed below are some typical signals:

- o High peak power short pulse with pulse widths typically in the order of 8 femtosecond to 2 picoseconds with a repetition rate as high as 100 MHz
- o Low level continuous wave light
- o Microwave modulated light transmitted through a fiber optic link which consists of three basic elements: a transmitter that converts an input broadband microwave signal to a modulated optical signal, a fiber optic transmission line, and a receiver to demodulate the modulated optical signal and provide a broadband microwave output signal.

Semiconductor lasers will probably emerge as the most desirable optical source because of their small size. Modulation of these semiconductor lasers can be performed externally and directly. It appears that direct modulation will be preferred because of its simplicity and lower driver power requirements. Because of development of the many high speed devices, it seems that fiber links with bandwidths greater than 10 GHz will be available in the near future. Phase array antenna performance can be enhanced in the future since these antennas are potential users of the technology of microwave links.

6.4 DIGITAL

Based upon technical data collected, survey information, related studies, and current technical literature, the following interpretations and projections regarding digital technology were made.

GaAs IC technology has progressed to the point where SSI and MSI circuits, with gate delays as low as 30 psec, are available for use in high-speed digital systems, while in the laboratory GaAs MOSFET gate delays as low as 5.8 psec have been obtained. Also, with the availability of the GaAs wafer foundation, the stage is set for the fabrication of high-speed digital ASIC design. System designers are currently taking advantage of faster and faster GaAs IC's and will to continue to do so in the future.

Chips are being fabricated with geometry features as small as 0.5 μm and a performance figure-of-merit of 1×10^{13} gate-Hz/cm^2 with a clock rate of 100 MHz. These geometry features and performance figures should ensure the introduction of the latest high technology components in military systems in six years and the insertion of some new technology into existing systems in the same time frame.

The next fo ır to six years will also bring the need to further modernize and improve existing weapons systems and drive the further development of MIMIC, ASIC, VHSIC, BiCMOS/CMOS, and GaAs technology. Actually, the MIMIC program was established to provide such modernization. GaAs MIMIC's from this program should complement VHSIC in many systems. For example, the design and fabrication of hybrid MIMIC would allow interface and communication between digital VHSIC and the RF analog world. It is likely that digital technology will go beyond the 100 MHz range because of MIMIC technology. Overall, digital systems using the emerging technology of 1990 through the year 1996 will operate at higher clock frequencies and data rates, consume less power, contain faster memories, and use faster microprocessors. Key technical parameters are forecasted below:

6.4.1 MICROPROCESSOR AVERAGE INSTRUCTION RATE (Reference: Figure 6-23 on page 6-41)

As with other microprocessor parameters, the average instruction rate as depicted in the trend curve is increasing. The trend shows that from 1976 to the present, the instruction rate increased from approximately 0.5 to 20 million instructions per second (MIPS). Current R&D efforts are expected to develop microprocessors with average instruction rates of 50 MIPS by 1996. SDI R&D efforts are setting 100 MIPS as a goal for microprocessor instruction rates which should be achievable by the end of the decade.

6.4.2 MAXIMUM DIGITAL LOGIC CLOCK FREQUENCY (Reference: Figure 6-24 on page 6-42)

The driving technologies for the high speed digital clock rates appear to be the GaAs and MIMIC component R&D efforts. Currently, GaAs technology is producing digital medium-scale integrated circuits which operate with clocks rates up to 10 GHz. By the year 2000, analog and digital interfacing requirements for MIMIC should push digital clock rates to the 30 GHz range to keep pace with MIMIC development efforts.

6.4.3 RAM ACCESS TIME (Reference: Figure 6-25 on page 6-43)

The technology trend from 1976 to the present depicts an ever decreasing access time for the various sizes of the four technologies of dynamic and static RAMs: NMOS, CMOS, ECL, and depletion mode. On the basis of the historical data, the technological survey, and the present amount of R&D being performed in industry today, it is expected that RAM access

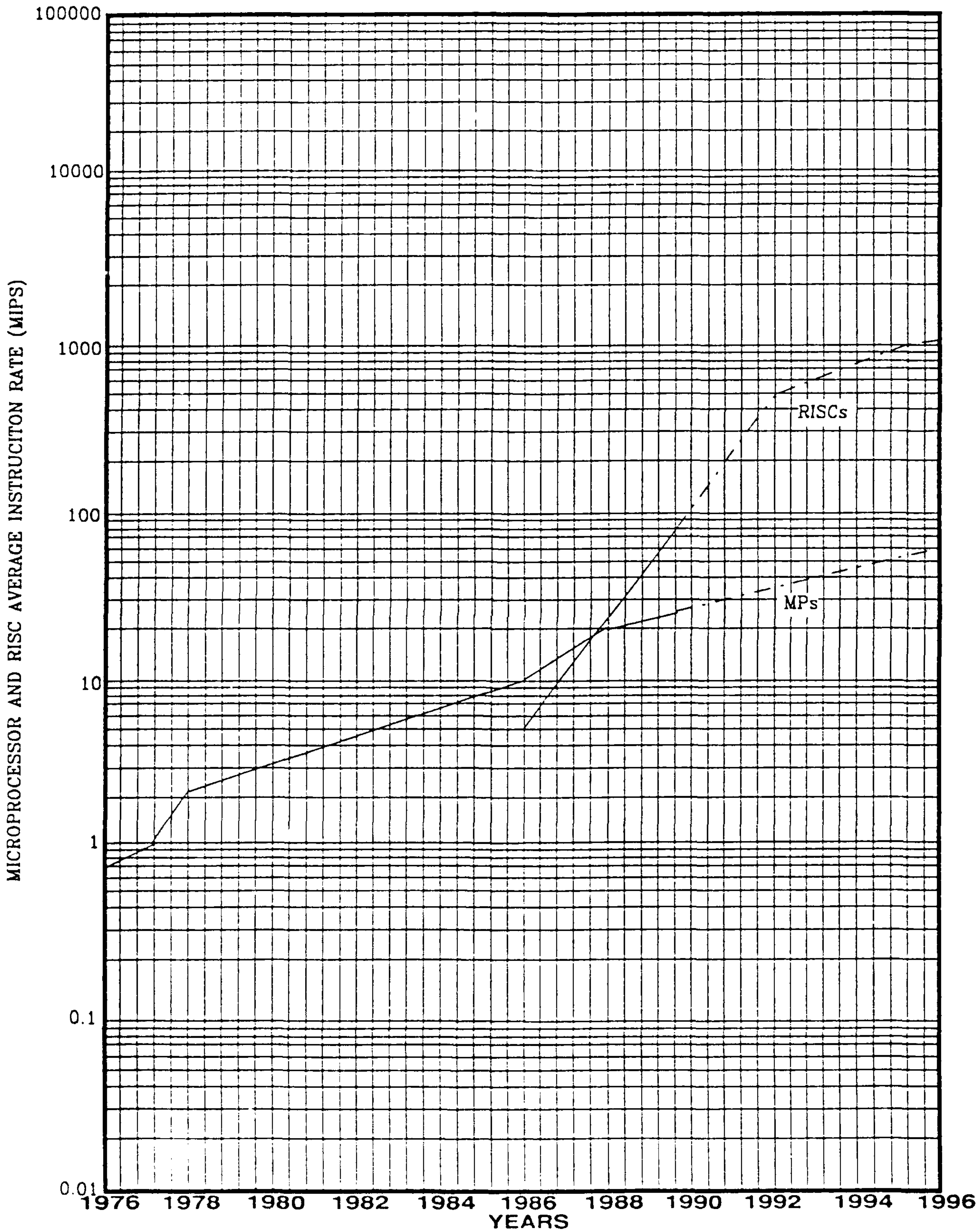

FIGURE 6-23. TREND CURVE FOR MICROPROCESSOR AND RISC SYSTEM AVERAGE INSTRUCTION RATE

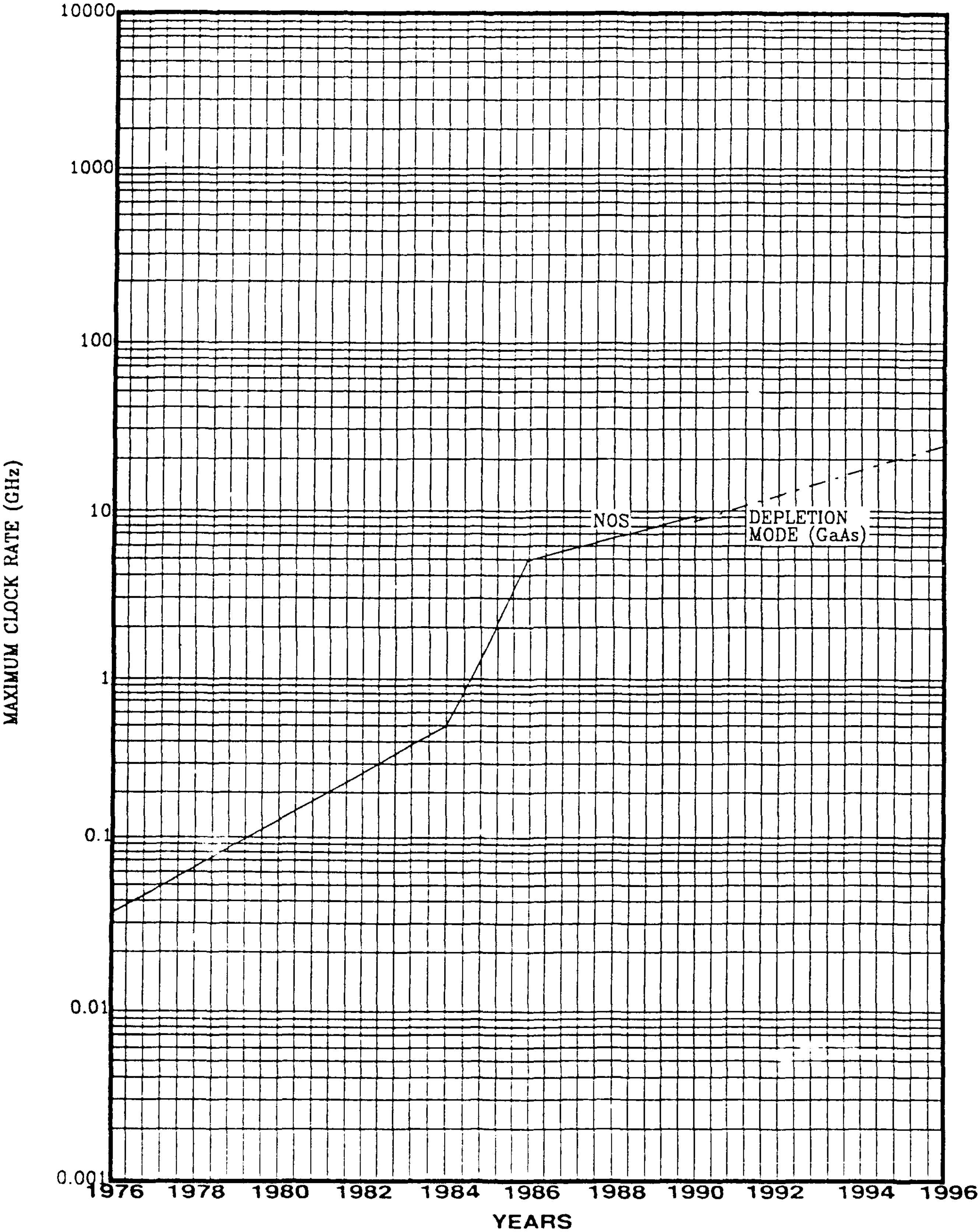

FIGURE 6-24 TREND CURVE FOR MAXIMUM DIGITAL LOGIC CLOCK FREQUENCY

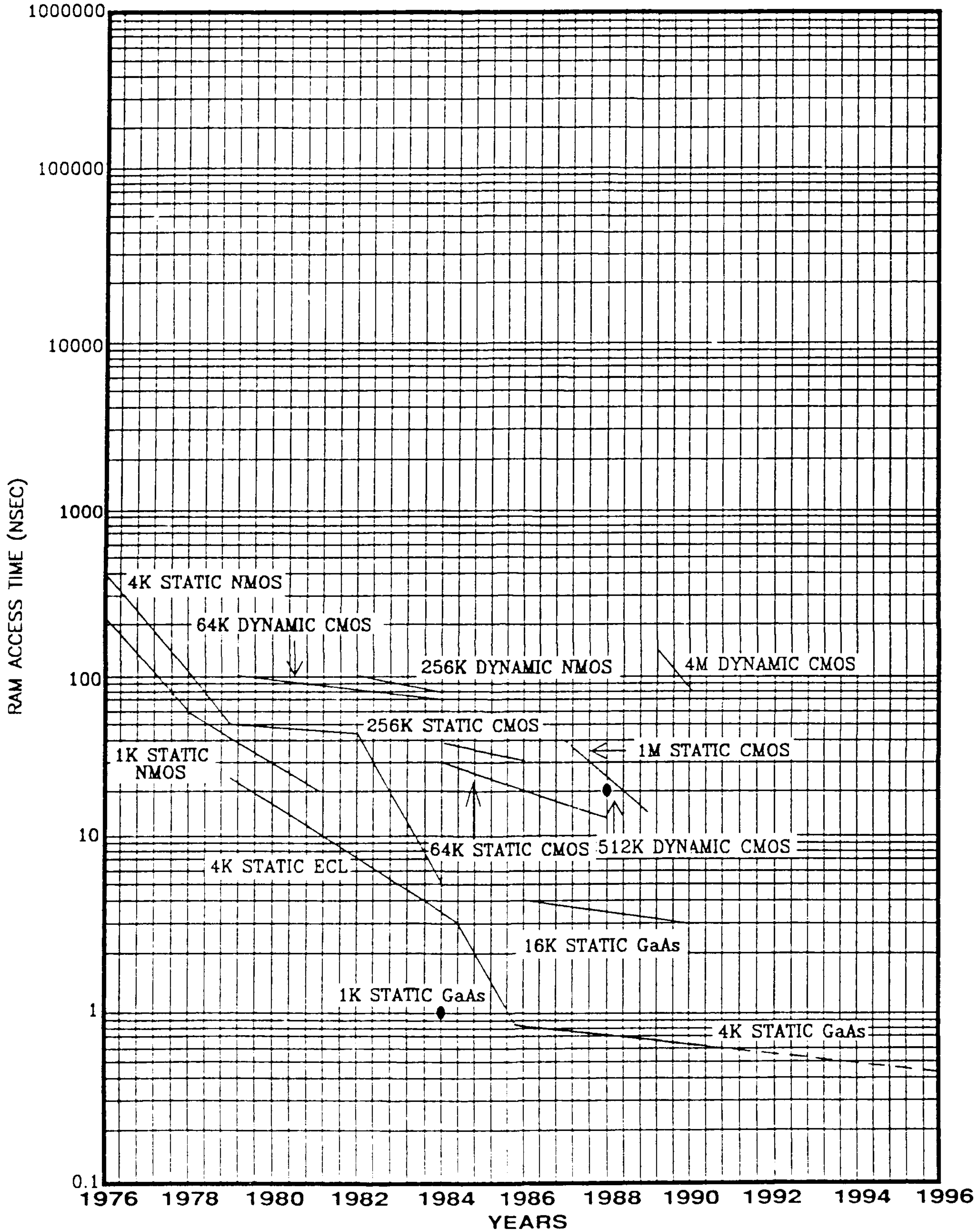

FIGURE 6-25. TREND CURVE FOR RAM MINIMUM ACCESS TIME

times for all memory sizes will continue to decrease in the future. Probably the 4K or less GaAs static RAMs will have access times of less than 550 psec by the end of this decade.

6.4.4 RAM BIT DENSITY (Reference: Figure 6-26 on page 6-45)

The RAM bit density technology trend from 1976 to the present depicts continued growth in both the dynamic and static RAM IC's. The current pattern appears to be for the DRAM bit density to quadruple about every four years with static RAM sizes following four years behind. This pattern is expected to continue until the end of the decade, producing DRAMS of 64M bits per chip and static RAMs of 16M bits per chip.

6.4.5 MICROPROCESSOR WORD LENGTH (Reference: Figure 6-27 on page 6-46)

In the past, as the demand to handle and solve complex problems utilizing voluminous amounts of data in a reasonable period has increased, single chip microprocessor CPU word length has also increased up to 32-bits. However, the development of the 64-bit single microprocessor chip has been delayed, according to industry survey consensus, because the 32-bit architecture is accepted as sufficient for all levels of computing until the end of the decade. It is expected that, by the next century, applications such as expert systems, speech/natural language processing, vision processing, and hologram imaging will create a high demand for the single 64-bit addressing microprocessor. Also, increased number crunching power will be made possible through advances in technology and design improvements which will enable microprocessors of tomorrow to operate at the order of tens (20-100) of MIPS, particularly with the advent of the Reduced Instruction Set Computers (RISCs).

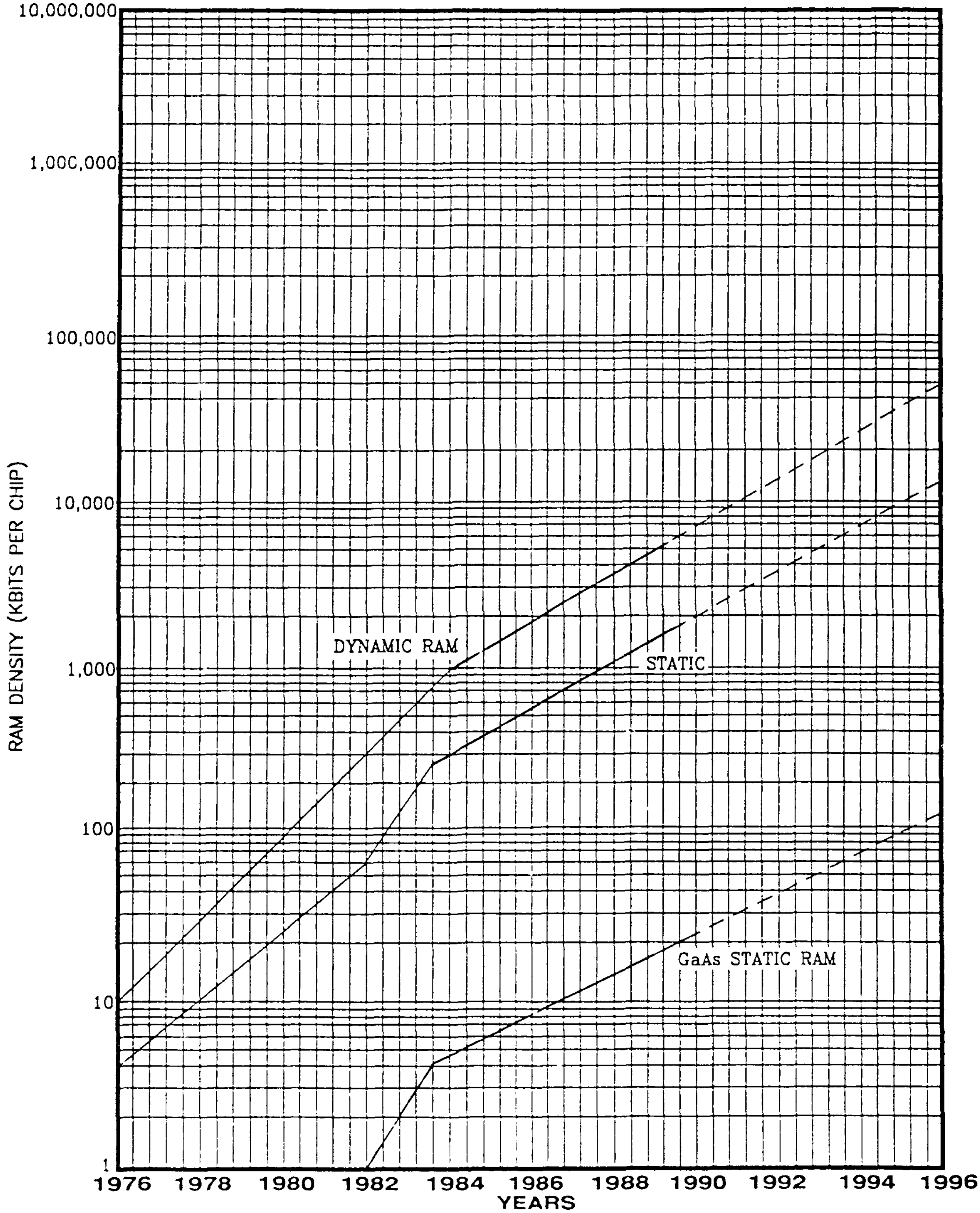

FIGURE 6-26. TREND CURVE FOR MAXIMUM RAM DENSITY

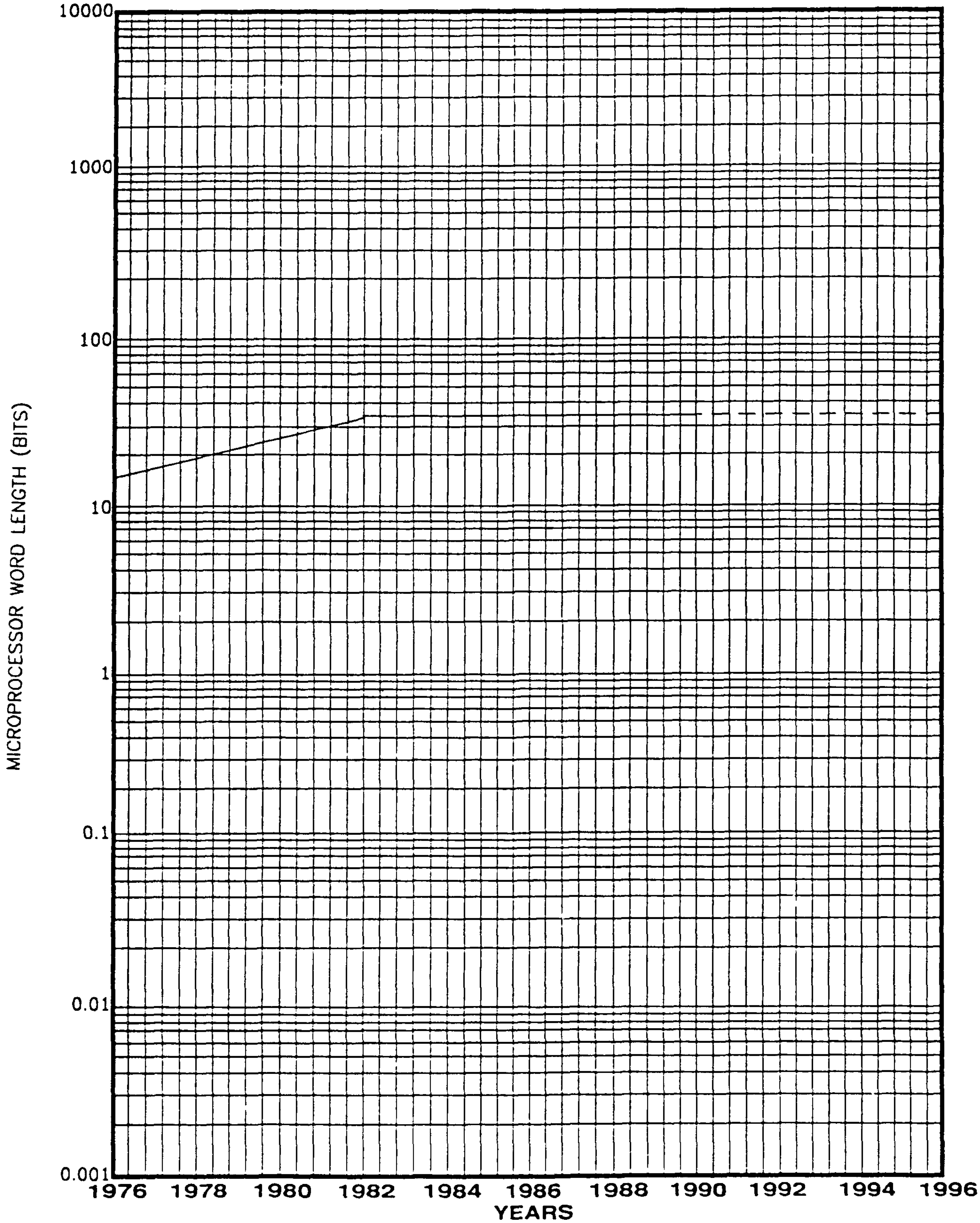

FIGURE 6-27. TREND CURVE FOR MICROPROCESSOR MAXIMUM WORD LENGTH

6.4.6 MICROPROCESSOR CLOCK FREQUENCY (Reference: Figure 6-28 on page 6-48)

Since the advent of the microprocessor, microprocessor clock rates have been increasing in order to decrease computation time and instruction execution time. R&D efforts, for example those of Defense Advanced Research Project Agency (DARPA), are looking into producing GaAs microprocessors that run at hundreds of megahertz per second (e.g., 200 MHz). Based upon prior history it is reasonable to expect that high speed microprocessors will be available within the next six years, at least in limited quantities.

6.4.7 DIGITAL GATE DELAYS (Reference: Figure 6-29 on page 6-49)

Over the years, digital gate delays have shown a steady decrease where GaAs technology has enabled the production of SSI chips with an average of 30 psec gate delays. Already in the laboratory, GaAs gate delays as low as 5.8 psec have been obtained. Thus, in six years such high speed SSI should be available for IC production.

6.4.8 BUBBLE MEMORY (Reference: Figure 6-30 on page 6-50)

Because the military and telecommunication industries have made heavy investments in their development, bubble memories are expected to remain in use at least until the end of the decade. However, for bubble memory use to be expanded, it will probably take an unforseen breakthrough in such capabilities as access times, as compared to those of ROM and RAM memories. Presently, 16 million bit chips are available. It is projected that several million bit chips will be available by the late 1990's.

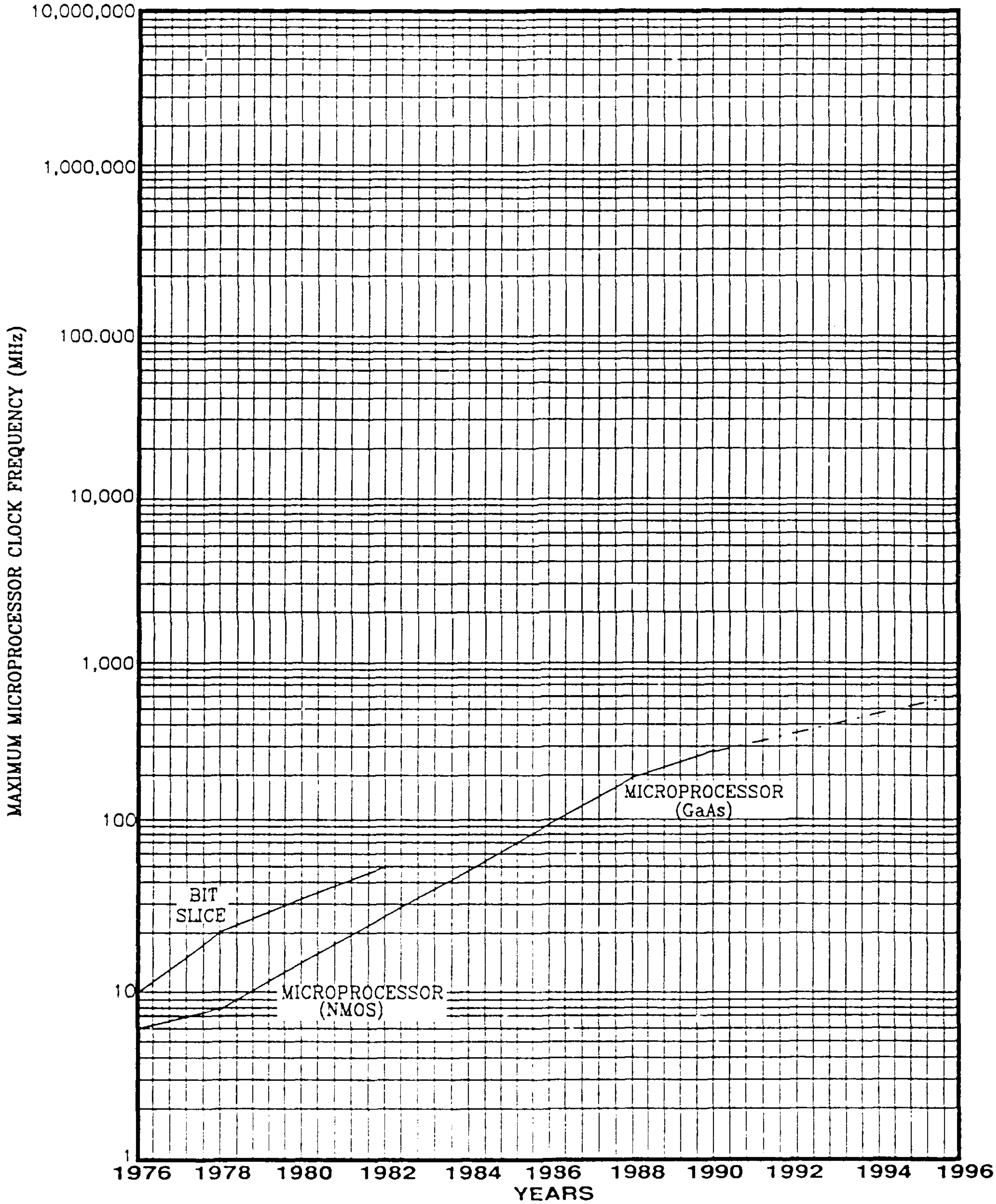

FIGURE 6-28. TREND CURVE FOR MICROPROCESSOR CLOCK FREQUENCY

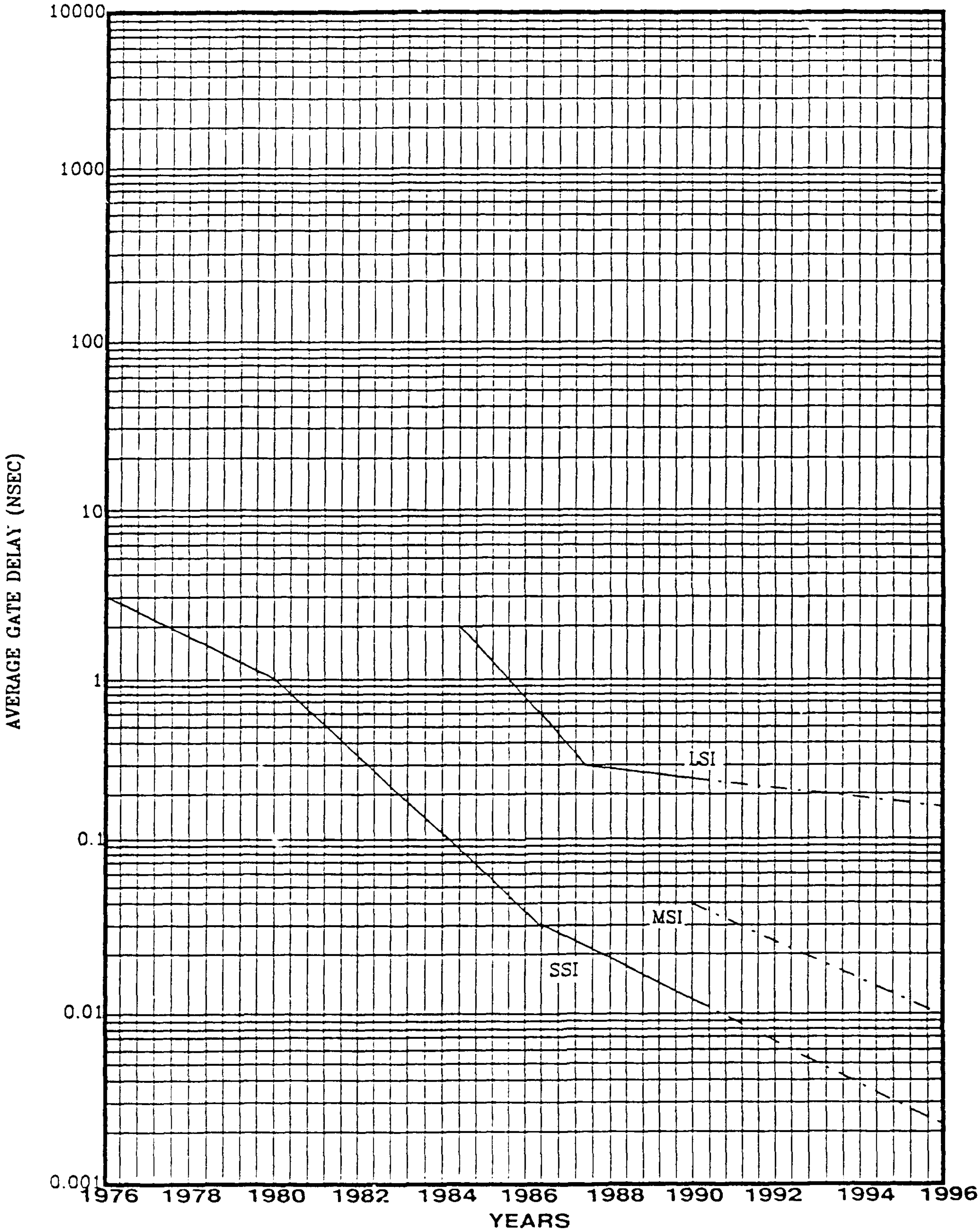

FIGURE 6-29. TREND CURVE FOR DIGITAL GATE DELAYS

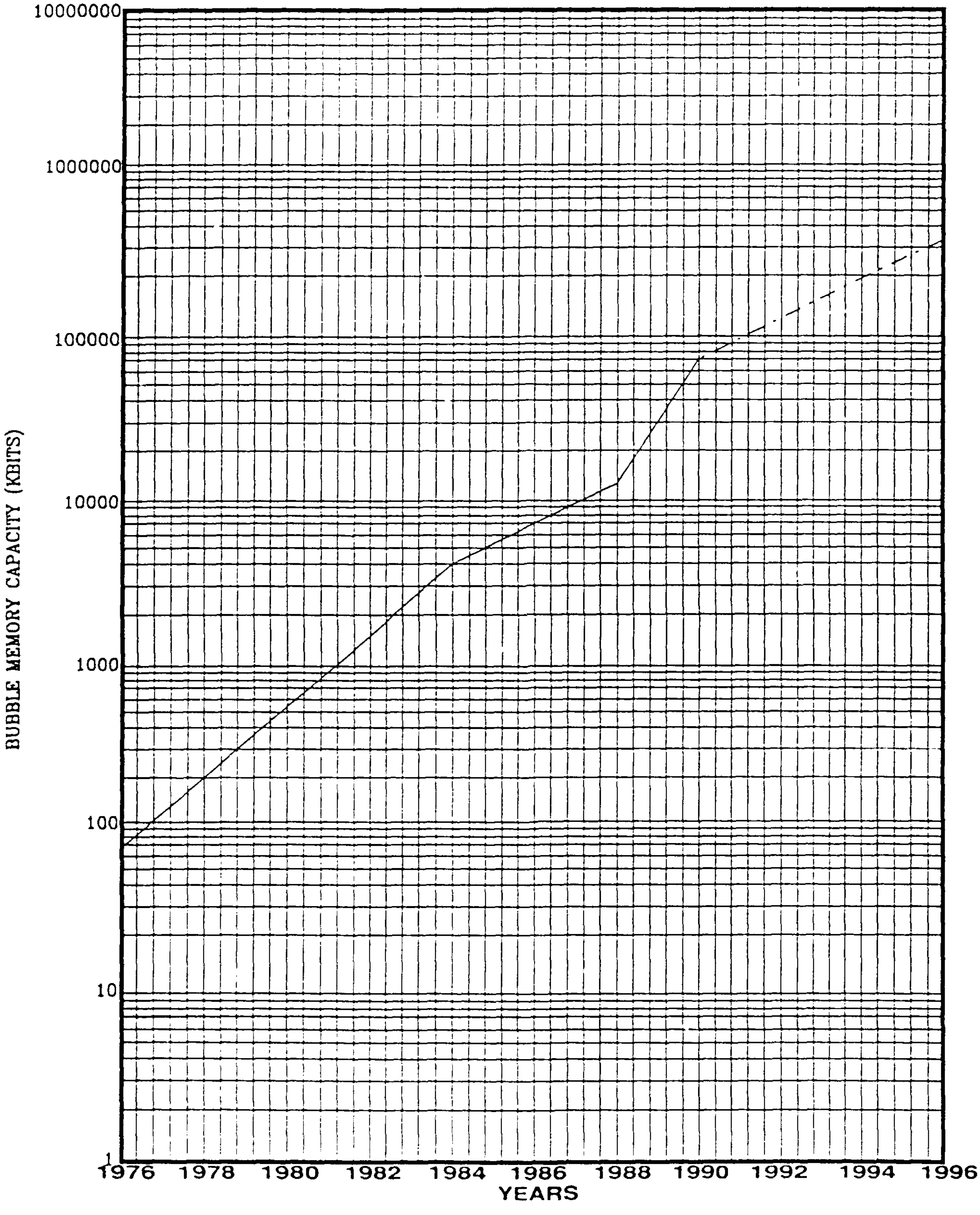

FIGURE 6-30. TREND CURVE FOR MAXIMUM BUBBLE MEMORY CAPACITY

6.4.9 LOGIC FAMILY OBSOLESCENCE (Reference: Figure 6-31 on page 6-52)

Because military logic life cycles are substantially longer than commercial industry life cycles, the military have designs in use that commercial equipment manufacturers would consider obsolete. Typically, militarization of commercial digital components can take up to two years. Acceptance by original equipment manufacturers of new logic families can take another two to five years, and military system designs may be based on logic families that are 15 years old. This lag between commercial and military technology was evident by the age of the electronic components in some of the Air Force equipment sampled. A long-term solution to the problem is the replacement of outdated technology with a newer technology. For example, such an update is planned for the F-15 aircraft. This move to newer technology can be projected using business sales projections of military logic components suppliers. The obsolescence of technology is indicated by the declining dollar value of the military supplier business, as shown in Figure 6-31 on page 6-52. On the other hand, the rising dollar value of military supplier business indicates projected use of the newer logic family technologies in the military equipment designs.

In general, a key digital technology, Application Specific Integrated Circuits (ASIC's), is the trend of future digital designs and will have great impact on digital technology because ASIC's will improve performance and reliability by putting more function on-chip and reducing the number of boards required in a system. Industry is currently creating a large library of standard cells around existing functional standards that include programmable logic families, 32-bit microprocessors, and error-correcting code modules. Today, the majority of ASIC's are designed with one μm-two μm geometries using CMOS. The present gate count on these ASIC's is in the order of 70,000, where as recently as 1984 a 10,000 gate count was maximum. ASIC's with propagation delays of one nsec are currently available.

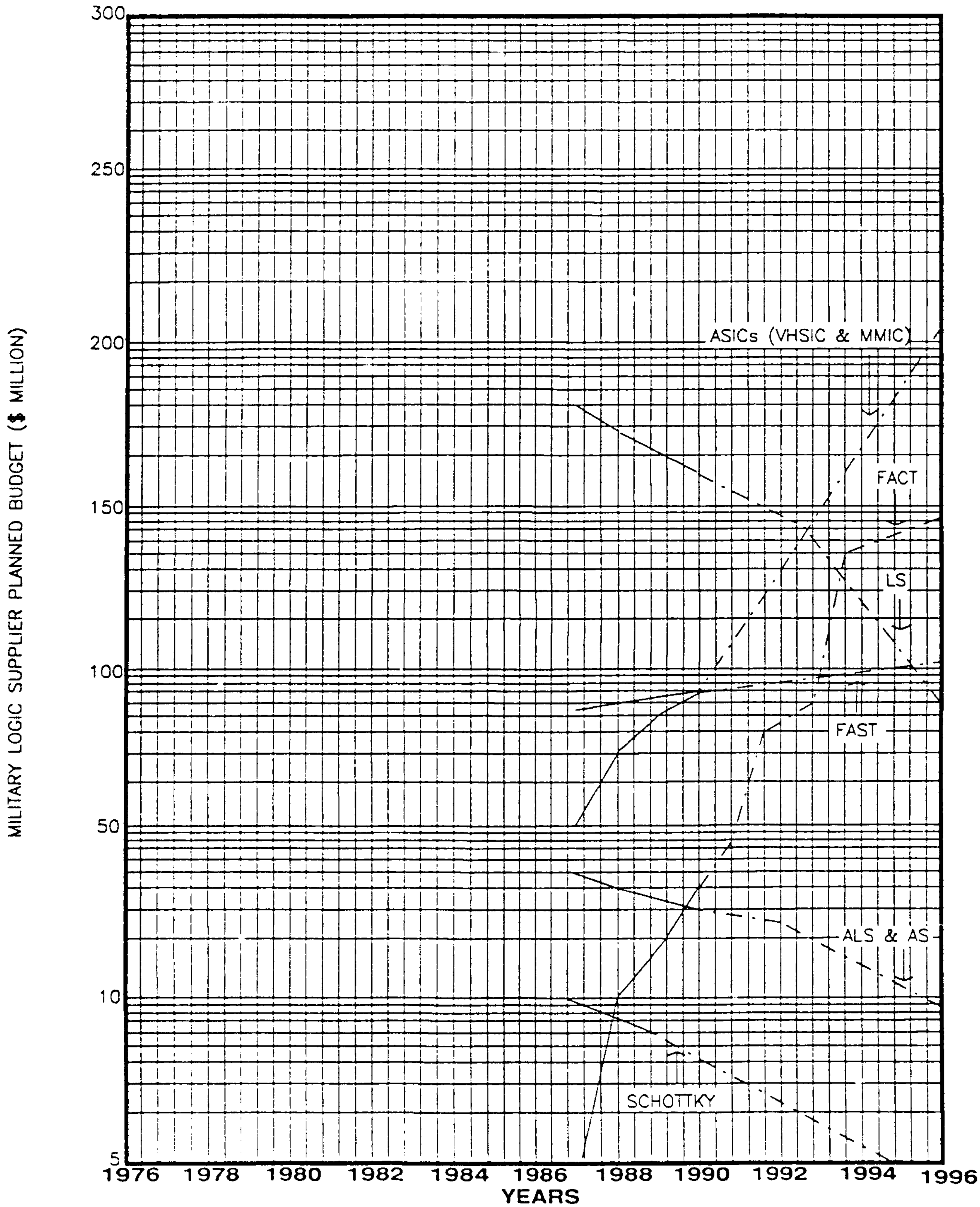

FIGURE 6-31. TREND CURVE FOR MILITARY LOGIC FAMILY OBSOLESCENCES.

Another ASIC technology trend that is considered important is the combination of RAM cells with ECL logic gates. It is expected that ASIC gate counts will increase to the hundreds of thousands, and their propagation delays will drop below 500 psec with geometries of 0.5 μm using BiCMOS technology that will increase operating frequency to the GHz range.

Furthermore, because of the digitalization trends pointed out in this section, industry is looking into developing a mixed analog and digital cell library with the idea of producing ASIC Digital Signal Processor (DSP). Because the DSP approach performs signal manipulation and analysis together at high operating speeds, the DSP has become a central player in areas where analog signal processing has long been dominant. Military applications of the DSP include such equipment as digital radios and radar systems. Typical DSP's may contain on-chip ROM with up to 32 thousand memory locations with a cycle time as low 37 nsec. The trend will be to provide more on-chip memory and decrease cycle time.

6.5 PCB TESTER FIXTURING

With the present technology trend of designing PCB's with ever increasing complexity and higher-speed circuits, PCB tester fixturing design is becoming more and more important. At high test frequencies, the transmission path shapes digital signals, and the line-to-line skew of digital signals can compromise critical pulse-edge timing. Test engineers must, therefore, consider transmission-line effects when fixturing test signals above 25 MHz. The fixturing should emulate, as nearly as possible, the real-world environment of the Device Under Test (DUT).

The creation of this real-world environment for DUT's involves addressing the following fixture or interface design issues:

- Control impedance interface: Provide cut-off frequency > 25 GHz to support edge rates in the 100 ps range
- Match line lengths: minimizes line-to-line skew
- Match line impedance: reduces VSWR
- Eliminate sharp bends, line width changes, and anomalies in the dielectric material: reduces reflection through line discontinuities.
- Minimize spurious capacitances: reduces loading down of signals
- Avoid stub lines: reduces VSWR
- Avoid close parallel traces: reduces crosstalk
- Keep trace spacing wide with respect to dielectric thickness: reduces crosstalk
- Minimize series resistances and reactances between signal paths and power sources or ground: reduces noise

In the future, the improper design of PCB tester fixtures for DUT interfaces will more and more often result in disappointing performance of both the tester and DUT. Careful attention to fixture or interface transmission line behavior will permit the accurate test of DUT's requiring high frequency and high quality signals.

APPENDIX A

AIR FORCE ELECTRONIC AND RELATED EQUIPMENT INVESTIGATED
(Reference Paragraph 2.1)

AIR FORCE ELECTRONIC AND RELATED EQUIPMENT INVESTIGATED

ITEM NO.	EQUIPMENT	FUNCTION	ARMED FORCES RESPONSIBLE	DATA SOURCE
01	AN/ALR-62	Countermeasures Receiving Radar	Air Force	Schematics Technical Data
02	AN/APQ-171	Terrain Following Radar	Air Force	Schematics Technical Data
03	AN/ALQ-184	Special Purpose Radar	Air Force	Schematics Technical Data
04	AN/FBS-117	Fixed Inactive Detection/Range/ Bearing	Air Force	Schematics
05	AN/ALQ-161A	Special Purpose Countermeasures	Air Force	Schematics Technical Data
06	AN/MPQ-T3	Transportable Special Purpose Radar	Air Force	Tester Envelope
07	AN/GPN-20	Navigation Radar	Air Force	Tester Envelope
08	AN/GPN-24	Navigation Radar	Air Force	Tester Envelope
09	AN/GPN-12	Navigation Radar	Air Force	Tester Envelope
10	AN/TRV-170V	Transportable Radio Communication	Air Force	Tester Envelope
11	AN/FYQ-93	Fixed Special Purpose Data Processing	Air Force	Tester Envelope
12	AN/VRC-83	Vehicular Radio Communications	Air Force	Tester Envelope
13	AN/PRC-113	Portable Radio Communication	Air Force	Tester Envelope

AIR FORCE ELECTRONIC AND RELATED EQUIPMENT INVESTIGATED (Cont'd)

ITEM NO.	EQUIPMENT	FUNCTION	ARMED FORCES RESPONSIBLE	DATA SOURCE
14	AN/GRC-206V (PACER SPEAK)	Ground Radio Communication	Air Force	Tester Envelope
15	AN/TPN-19	Transportable Navigation Radar	Air Force	Tester Envelope
16	AN/TPQ-43	Transportable Special Purpose	Air Force	Tester Envelope
17	AN/TSQ-111V	Transportable Special Purpose/ Special Type	Air Force	Tester Envelope
18	AN/GSC-37	Ground, Special Type Communica- tion	Air Force	Tester Envelope
19	AN/GSC-38	Ground, Special Type Communica- tion	Air Force	Tester Envelope
20	AN/ALQ-172	Countermeasures	Air Force	Interview Survey
21	MRT	Miniature Receive Terminal	Air Force	Schematics Technical Data
22	AN/APX-103	IFF (E3-A)	Air Force	Tester Envelope
23	AN/ALQ-131	EW Jamming Pod	Air Force	Schematics Technical Data
24	VCC	F-15 Central Computer	Air Force	Schematics Technical Data
25	AN/APY-1/2	(E3-A) Surveillance Radar	Air Force	Schematics Technical Data
26	AN/AAQ-114	(LANTIRN) Special Purpose Infrared	Air Force	Schematics Technical Data

AIR FORCE ELECTRONIC AND RELATED EQUIPMENT INVESTIGATED (Cont'd)

ITEM NO.	EQUIPMENT	FUNCTION	ARMED FORCES RESPONSIBLE	DATA SOURCE
27	CNCE	Communications	Air Force	TRDs[1]
28	JTIDS	Joint Tactical Info Distribution System	Joint	Interview Survey
29	MILSTAR	Satellite Communications	Joint	Schematics Technical Data
30	AEGIS	Defensive	Navy	TRDs
31	AN/SPN-42A	(Water) Navigation Radar	Navy	See Note 2
32	AN/SLQ-32	(Water) Special Purpose Countermeasures	Navy	See Note 2
33	AN/SQS-53	(Water) Sonar Detection/Range/Bearing	Navy	See Note 2
34	AN/SPN-43A	(Water) Navigation Radar	Navy	See Note 2
35	AN/VQX-5	(Utility) Identification and Recognition Sonar	Navy	See Note 2
36	AN/UYK-44	(Utility) Data Processing Computing	Navy	See Note 2
37	AN/UYK-20	(Utility) Data Processing Computing	Navy	See Note 2
38	AN/SPS-48(V)	(Utility) Data Processing Computing	Navy	See Note 2

1. TRD - Test Requirement Document

2. Reference W. Schmitt's NAVSEA Report in Appendix D on page D-7

AIR FORCE ELECTRONIC AND RELATED EQUIPMENT INVESTIGATED (Cont'd)

ITEM NO.	EQUIPMENT	FUNCTION	ARMED FORCES RESPONSIBLE	DATA SOURCE
39	AN/UYK-7	(Utility) Data Processing Computing	Navy	See Note 2
40	AN/WSN-5	(Water) Special Type Navigation	Navy	See Note 2
41	AN/WSN-2	(Water) Special Type Navigation	Navy	See Note 2
42	AN/SPG-55B	(Water) Fire Control Radar	Navy	See Note 2
43	AN/WRL-8	(Water) Radio Searchlight Control	Navy	See Note 2
44	MK-91	Fire Control	Navy	See Note 2
45	MK-15	Identification Friend or Foe	Navy	See Note 2
46	MK-92	Fire Control	Navy	See Note 2
47	PAWS	Smart Video Processor/ Computer Terminal	Army	PCB Schematics
48	FSIC	Crypto Communication and Disk Storage	Army	PCB Schematics
49	AIM	Fiber Optic Data/Voice Communication	Army	PCB Schematics

APPENDIX B

PCB TESTER SURVEY FORM

(Reference paragraph 3.2.1)

PCB TESTER SURVEY DATA COLLECTION SHEET

System Name: ____________ Manufacturer: ____________

System Ident.No.: ____________

GENERAL

System Type: ____________

____

Applications Range: ____________

System Status/Age: ____________

Portability: ____________

Cost: ____________

CONTROL SUBSYSTEM

Controller Type: ____________

Mfr/Model No.: ____________

Memory: ____________

Mass Memory: ____________

____

System Peripherals: ____________

____

Test Adapter Implementation Characteristics: ____________

Physical Description: ____________

Size: ____________

Weight: ____________

Sheet___of___

PCB TESTER SURVEY DATA COLLECTION SHEET (Cont'd)

System Name: ____________________

System Ident.No.: ______________

System Software: ____

Training Available: ____

Other Manufacturer Services: _________________________________

____

Programming Complexity & Characteristrics: ___________________

Operation and Use Requirements: ______________________________

Performance Upgrading Capability: ____________________________

PCB TESTER SURVEY DATA COLLECTION SHEET (Cont'd)

System Name:__________________

System Ident.No.:_____________

POWER SOURCES AND STANDARDS
DC VOLTS, DC CURRENT, AC POWER

No.	Type	V Range/Steps	I Range/Steps	AC Only - # Phase/Freq-Range/Freq-Steps

Sheet___of____

PCB TESTER SURVEY DATA COLLECTION SHEET (Cont'd)

System Name:________________

System Ident.No.:____________

ANALOG STIMULI

No.	Waveshape and Type	Freq Range/Steps	Ampl Range/Steps	Spec Function Type Range/Steps	Modulation

SPECIAL STIMULI

No.	Type	Description

Sheet___of___

PCB TESTER SURVEY DATA COLLECTION SHEET (Cont'd)

System Name: ____________

System Ident.No.: ____________

ANALOG RESPONSE

No.	Type/Function	Range	Accuracy/Resolution

SPECIAL RESPONSE

No.	Type/Function	Description

Sheet ___ of ___

PCB TESTER SURVEY DATA COLLECTION SHEET (Cont'd)

System Name:________________

System Ident.No.:____________

DIGITAL

QUANT	Dynamic Stimuli	CHARACTERISTICS MIN	MAX	RES	UNITS	LIMITS	MAX	I/O		CLOCK	PIN MEMORY
	LOGIC 1					Vp-p		STIM ☐	RESP ☐	INT ☐	STIM
	LOGIC 0					VxF		BI-DI ☐	TRI-S ☐	EXT ☐	RESP
	FREQ					Bits (wd)		SER ☐	PAR ☐		
						Bits (tot)					

QUANT	Static Stimuli	CHARACTERISTICS MIN	MAX	RES	UNITS	LIMITS	MAX	I/O		CLOCK	PIN MEMORY
	LOGIC 1					Vp-p		STIM ☐	RESP ☐	INT ☐	STIM
	LOGIC 0					VxF		BI-DI ☐	TRI-S ☐	EXT ☐	RESP
	FREQ					Bits (wd)		SER ☐	PAR ☐		
						Bits (tot)					

QUANT	Static Reponse	CHARACTERISTICS MIN	MAX	RES	UNITS	LIMITS	MAX	I/O		CLOCK	PIN MEMORY
	LOGIC 1					Vp-p		STIM ☐	RESP ☐	INT ☐	STIM
	LOGIC 0					VxF		BI-DI ☐	TRI-S ☐	EXT ☐	RESP
	FREQ					Bits (wd)		SER ☐	PAR ☐		
						Bits (tot)					

Sheet___of____

APPENDIX C

PCB DATA SHEET

(Reference paragraph 3.2.1)

UUT CLASSIFICATION/FUNCTIONAL TEST REQUIREMENTS SUMMARY

PAGE__ OF__

MFR. NAME ________________ TRD NO. ________________

UUT NAME ________________ REV. ________________

NSN OR PART NO. ________________ DATE ________________

REF.DES. ________________

CLASSIFICATION DESCRIPTOR			
DIGITAL FUNCTION		RF/ANALOG FUNCTION	
DIGITAL TECHNOLOGY		RF/ANALOG TECHNOLOGY	

FUNCTIONAL TEST REQUIREMENTS SUMMARY

	STIMULUS	
DIGITAL	DYNAMIC	
	STATIC	
	LOGIC TYPE	
	I/O CHARS	
	SIMULT. I/O REQ.	
PWR	DC	
	AC	
ANALOG	SINE	
	SQUARE	
	TRIANGLE	
	SAWTOOTH	
	PULSE	
	ARBITRARY	
RF	CW	
	AM	
	SSB	
	SCM	
	FM	
	PULSE	
SPECIAL	SYNCHRO	
	RESOLVER	
	LASER	
	PRESSURE	
	OTHER	
LOAD	R	
	L	
	C	
	COMPLEX	

	RESPONSE	
DIGITAL	DYNAMIC	
	STATIC	
	LOGIC TYPE	
	I/O CHARS	
	SIMULT. I/O REQ.	
VOLTAGE	DC	
	AC	
	RFV	
	RFP	
	SAMPLED	
F/T	FREQ.	
	TIME INT.	
ANAL	WAVAN	
	SPECAN	
	FFT	
RFDEMOD	AM	
	SSB	
	SCM	
	FM	
	PULSE	
SPECIAL	SYNCHRO	
	RESOLVER	
	LASER	
	PRESSURE	
	OTHER	
Z	R	
	L	
	C	
	COMPLEX	

NOTES	

APPENDIX D

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APPENDIX E

SURVEY QUESTIONNAIRE
(Reference paragraph 3.2.5.1)

TECHNOLOGY SURVEY QUESTIONNAIRE

Based upon your knowledge of VSHIC, MMIC, or Planned System Technologies, enter any known planned parametric ranges below for the listed attributes for each technology category:

Parametric Ranges Based On:____________________

Technology Category	Attributes	Planned Parametric Range
<u>Millimeter Wave</u>	1. Operating Frequency (GHz) 2. Bandwidth (Percent of Operating Frequency) 3. Solid-State Device Continuous Wave Output (Watts) 4. Output Power (Watts) 5. Mean Time Between Failures (Hours)	
<u>Spread Spectrum</u>	1. Frequency/Phase Agility (Frequency/Phase Changes /Second) 2. Acquisition/Synchronization time (Microseconds) 3. Maximum Bandwidth (Frequency Hopping or Suppressed Carrier) (Hertz) 4. Effective Radiated Power of Anti-Jamming Systems (Watts) 5. Bit Error Rate (Bit Errors /Second) 6. Mean Time Between Failures (Hours)	

TECHNOLOGY SURVEY QUESTIONNAIRE (Cont'd)

Technology Category	Attributes	Planned Parametric Range
Multiplex Bus (Electrical	1. Data Rate (M Bits/Second) 2. Network Size (Maximum Number of Nodes) 3. System Capacity (Maximum Number of Simultaneous Messages)	
Integrated Circuits/ Microprocessors	1. Operating Speed (Floating Point Operations/Second) 2. Memory Access Speed into a RAM (Nanoseconds) 3. Memory Capacity (Dynamic RAM) (Bits/Chip) 4. Density (Gates/Chip) 5. Package Size (Number of Connector Pins) 6. Integrated Circuit Mean Time Between Failures (Hours)	
Mass Data Storage	1. Density (Bits/Square Inch) 2. Transfer Rates (Bits/Second) 3. Mean Time Between Failures (Hours)	
Power	1. D.C. Voltage 2. D.C. Current 3. AC Voltage 4. AC Current 5. Phases 6. No. of Simultaneous Voltages	

TECHNOLOGY SURVEY QUESTIONNAIRE (Cont'd)

Technology Category	Attributes	Planned Parametric Range
Built-In Test	1. Faults Detected by BIT (Percent of Total Real Failures) 2. Faults Detected by BIT and Isolated to Shop Replaceable Assembly Level by BIT (Percent of Total Faults Detected by BIT) 3. BIT False Alarm Rate (Percent of Total BIT Fault Alarms) 4. BIT Versatility (e.g., Threshold Reprogrammability, etc.) (Percent of Total Avionics BIT that Is Reprogrammable) 5. BIT Continuous Monitoring (Percent of Avionics Having BIT Continuous Monitoring) 6. BIT Volume (Percent of Avionics Shop Replaceable Assembly Devoted to BIT)	
Fiber Optics	1. Network Size (Number of Nodes) 2. Network Capacity (Maximum Number of Simultaneous Messages) 3. Data Rate (Bits/Second) 4. Coupler Loss Variability (dB) 5. Receiver Sensitivity (dBm) 6. Transmitter Power (dBm) 7. Mean Time Between Failures (Hours)	

TECHNOLOGY SURVEY QUESTIONNAIRE (Cont'd)

Technology Category	Attributes	Planned Parametric Range
Fiber Optics (Cont'd)	8. Use of Fiber Optic Bus (Percent of All Avionics Buses that Are Fiber Optic) 9. Wavelength	
Displays	1. Data Rate (Pixels/Second) 2. Resolution (Pixels/Inch) 3. Brightness Under High Ambient Conditions (Foot-Lamberts) 4. Use of Color (Percent of Displays Having Color Capability) 5. Volume (Cubic Inches) 6. Mean Time Between Failures (Hours) 7. Power Consumption (Watts)	
High-Speed/High-Volume Digital Input/Output	1. Logic Levels 2. Clock Rate 3. Data Rate 4. Logic Mix 5. I/O Count 6. Sequenced Pattern Depths 7. Rise/Fall Time	
General Analog	SINE: 1. Frequency 2. Amplitude	

TECHNOLOGY SURVEY QUESTIONNAIRE (Cont'd)

Technology Category	Attributes	Planned Parametric Range
<u>General Analog</u> (Cont'd)	PULSE: 1. Frequency 2. Amplitude 3. Width 4. Rise/Fall Time 5. Power ARBITRARY WAVE: 1. Wave shape 2. Frequency 3. Amplitude RF: 1. Frequency 2. Power	

COMMENTS:

APPENDIX F
KEY PCB TESTER (ATE) SYSTEMS IDENTIFIED IN SURVEY
(Reference paragraph 3.2.5.2)

KEY PCB TESTER (ATE) SYSTEMS IDENTIFIED IN SURVEY

ITEM NUMBER	NAME	MANUFACTURER	TYPE	LOCATION
01	GAI 390	Giordano	Digital	Kelly AFB
02	GREENBRIER	Greenbrier	Digital	Kelly AFB
03	GR1796	GenRad	Hybrid	Kelly AFB Robins AFB McClellan AFB
04	GR2225	GenRad	Hybrid	Kelly AFB Robins AFB McClellan AFB
05	GR2235	GenRad	Digital	Kelly AFB Robins AFB McClellan AFB
06	GR2750	GenRad	Digital	McClellan AFB
07	IFTE	Grumman	Hybrid	Ft. Monmouth
08	TAT	Harris	Analog	Crane (Navy)
09	ADTS 2600	Honeywell	Analog	McClellan AFB Hill AFB
10	ATS-1000-RF	GE Aerospace	RF	Robins AFB McClellan AFB
11	OTH-B	GE Aerospace	RF/Hybrid	No Data
12	DATSA	Emerson	Hybrid	Kelly AFB Robins AFB McClellan AFB
13	HP9580A	Hewlett Packard	Microwave	McClellan AFB
14	AUGMENTED GR1796	GenRad/Air Force	Hybrid	McClellan AFB
15	L393	Teradyne	Digital	No Data
16	FACTRON 720	Schlumberger	Digital	No Data
17	HP9571A	Hewlett Packard	Digital	McClellan AFB

KEY PCB TESTER (ATE) SYSTEM IDENTIFIED IN SURVEY
(Cont'd)

ITEM NUMBER	NAME	MANUFACTURER	TYPE	LOCATION
18	CASS	GE Aerospace	1. CNI 2. EW 3. Radar 4. E/O 5. Digital 6. Hybrid	(Future Tester)
19	CA8200	Computer Automation	Digital	Kelly AFB
20	DTRS	GE Aerospace	Hybrid	No Data
21	ADINTS	Harris	Hybrid	Robins AFB
22	DTS-70	Hewlett Packard	Hybrid	McClellan AFB Robins AFB
23	AN/GSM-333	GEC	Hybrid	No Data

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